Control Integrated POwer System (CIPOS™)

AN-CIPOS mini-1-Technical Description

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1 Scope

The scope of this application note is to describe the product family of CIPOS™ and the basic requirements for operating the products in a recommended mode. This is related to the integrated components, such as IGBT or gate drive IC, as well as to the design of the necessary external circuitry, such as bootstrap or interfacing. Integrating discrete power semiconductors and drivers into one package allows them to reduce the time and effort spent on design. To meet strong demand for small size and higher power density, LS Power Semitech has developed a new family of highly integrated intelligent power modules that contain nearly all of the semiconductor components required to drive electronically controlled variable-speed electric motors. They incorporate a three-phase inverter power stage with a SOI gate driver and Infineon's leading-edge Trench Stop RC-IGBT except for IKCMxxx60xA. Trench Stop IGBTs and diodes are used for IKCMxxx60xA.

The application note concerns the following products.

IKCM30F60xA

IGCM20F60xA

IGCM15F60xA

IGCM10F60xA

IGCM06F60xA

IGCM04F60xA

IGCM06B60xA

IKCM10H60xA

IKCM15H60xA

IKCM20H60xA

CIPOS™ is family of intelligent power modules, which are designed for motor drives in household appliances, such as air conditioners, washing machines, refrigerators, dish washers and low power industrial applications as well.

1.1 Product line-up

Table 1. Line-up of CIPOS™

Part Number	Rating		Internal Circuit	Package	Isolation Voltage(Vrms)	Main Applications
	Current (A)	Voltage (V)				
IKCM30F60xA	30	600	3ϕ Bridge, Open emitter	Fully molded DIL module	2000Vrms Sinusoidal, 1min.	Air Conditioner Sewing machine
IGCM20F60xA	20					
IGCM15F60xA	15					Air Conditioner Washing Machine Sewing machine
IGCM10F60xA	10					
IGCM06F60xA	6					Refridgerator Dish Washer
IGCM04F60xA	4					
IGCM06B60xA	6		3ϕ Bridge & 1ϕ Rectifier, Closed emitter			
IKCM10H60xA	10		3ϕ Bridge, Open emitter			Washing Machine
IKCM15H60xA	15					
IKCM20H60xA	20					

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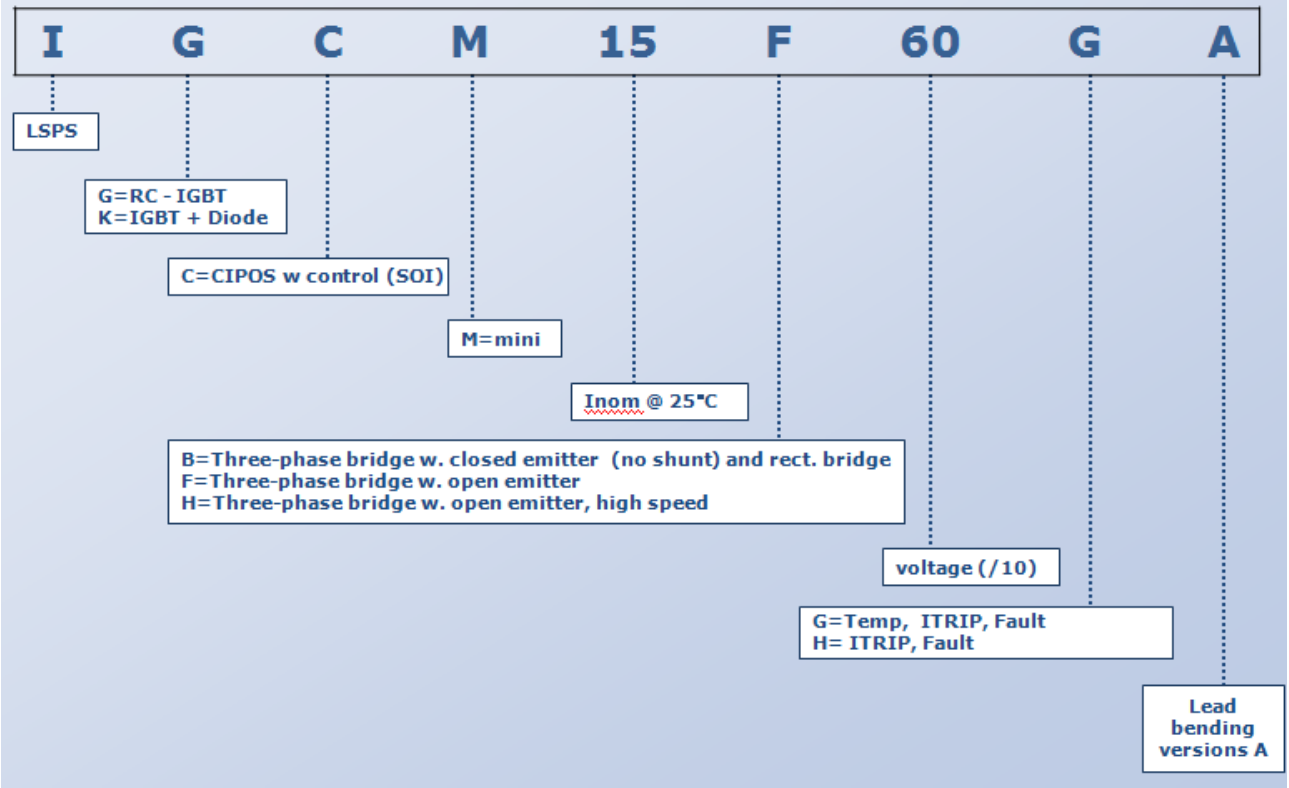
1.2 Nomenclature



2 Internal Components and Package Technology

2.1 Power transistor technology– Trench Stop IGBT and RC-IGBT

Infineon technologies introduced its Trench Stop IGBT technology in 2004 and RC-IGBT technology in 2007 [1].

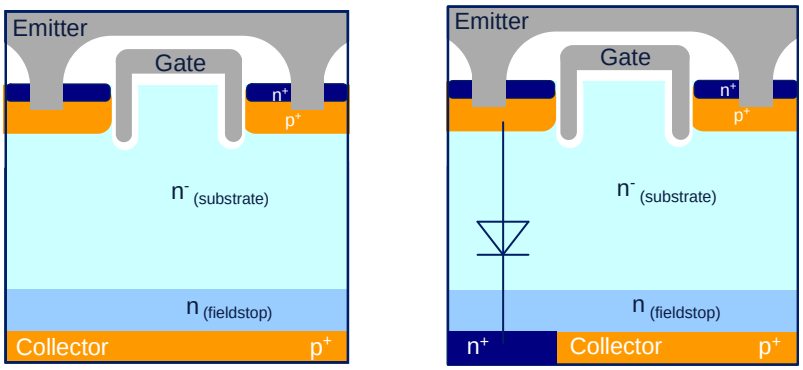


Figure 1. Cross section of Trench Stop IGBT (Left) and RC-IGBT (Right) cells

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The technology continues the well known properties of robustness of Infineon IGBT, such as short circuit withstand capability and maximum junction temperature. On the other hand all advantages of the technology remain in order to achieve highest efficiency and enable for highest power density. This refers to very low static parameters such as saturation voltage of IGBT or forward voltage of diode as well as to the excellent dynamic parameter such as turn-off energy of the IGBT or the reverse recovery charge of the diode.

2.2 Control IC – 6 channel gate drive IC

The basic feature of this technology is the separation of the active silicon from the base material by means of a buried silicon oxide layer as shown in Figure 2.

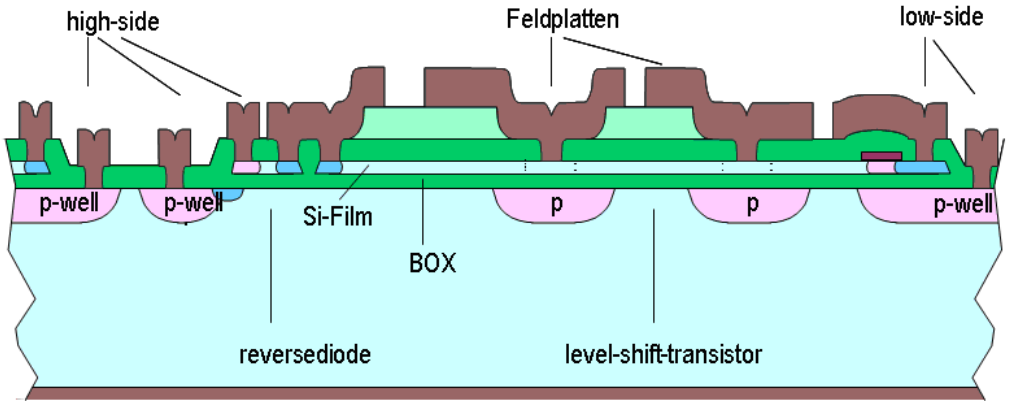


Figure 2. Cross section of a 6 channel gate drive IC cell

The buried silicon oxide provides an insulation barrier between the active layer and silicon substrate and hence reduces the parasitic capacitance tremendously. Moreover, this insulation barrier disables leakage or latch-up currents between adjacent devices. This prevents the latch-up currents between adjacent devices. This prevents the latch-up effect even in case of high dv/dt switching under elevated temperature and hence provides improved robustness. Besides the Thin-film SOI technology provides additional benefits like lower power consumption and higher immunity to radioactive radiation or cosmic rays [2]. A monolithic single control IC for all 6 IGBTs provides further advantages, such as bootstrap circuitry, matched propagation delay times, built-in deadtime, cross conduction prevention and all 6 IGBTs turn-off under fault situation like under voltage lockout and over current.

2.3 Thermistor

In case of I CIPOS™, thermistor is integrated on the internal PCB. It is connected between VFO and VSS. A circuit proposal for over temperature protection by using it is discussed in section 5.4.

Table 2. Raw data of CIPOS™ mini thermistor

T [°C]	Rmin [kΩ]	Rtyp [kΩ]	Rmax [kΩ]	Tol [%]	T [°C]	Rmin [kΩ]	Rtyp [kΩ]	Rmax [kΩ]	Tol [%]
-40	2662.292	2962.540	3262.789	10.1	45	34.520	36.508	38.496	5.4
-35	1925.308	2133.692	2342.076	9.8	50	28.400	29.972	31.545	5.2
-30	1407.191	1553.414	1699.637	9.4	55	23.485	24.735	25.985	5.1
-25	1038.949	1142.63	1246.312	9.1	60	19.517	20.515	21.514	4.9
-20	774.497	848.747	922.997	8.7	65	16.296	17.097	17.898	4.7
-15	582.690	636.369	690.048	8.4	70	13.670	14.315	14.960	4.5
-10	442.252	481.410	520.568	8.1	75	11.517	12.039	12.561	4.3
-5	338.491	367.303	396.114	7.8	80	9.745	10.169	10.593	4.2
0	261.164	282.537	303.910	7.6	85	8.279	8.625	8.971	4.0
5	203.056	219.036	235.016	7.3	90	7.062	7.345	7.628	3.9
10	159.044	171.081	183.118	7.0	95	6.046	6.279	6.511	3.7
15	125.454	134.586	143.717	6.8	100	5.199	5.388	5.576	3.5
20	99.630	106.605	113.580	6.5	105	4.468	4.640	4.811	3.7
25	79.638	85.000	90.362	6.3	110	3.856	4.009	4.163	3.8
30	64.055	68.203	72.352	6.1	115	3.338	3.477	3.615	4.0
35	51.831	55.059	58.287	5.9	120	2.900	3.024	3.149	4.1
40	42.182	44.708	47.235	5.7	125	2.527	2.639	2.751	4.2

2.4 Package technology

The CIPOS™ offers the smallest size while providing high power density up to 600V, 30A by employing Trench Stop IGBT + diode or RC-IGBT with 6 channel gate drive IC. It contains all the power components such as the IGBTs and isolates them from each other and from the heat sink. All the low power components such as the gate drive IC and thermistor (optional) are assembled on a PCB.

The electric insulation is given by the mold compound itself, which is simultaneously the thermal contact to the heat sink. In order to further decrease the thermal impedance, the internal lead frame design is optimized [3]. Figure 3 and Figure 4 show the external view and cross section of CIPOS™ package.

Figure 5 shows 2 kinds of internal lead-frame layouts.

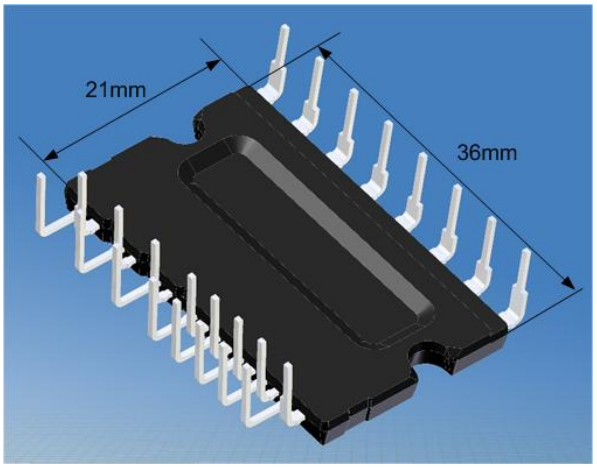


Figure 3. External view of CIPOS™

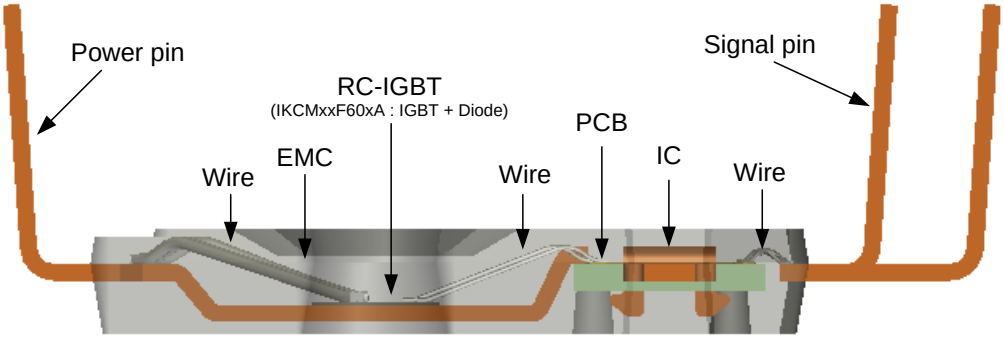
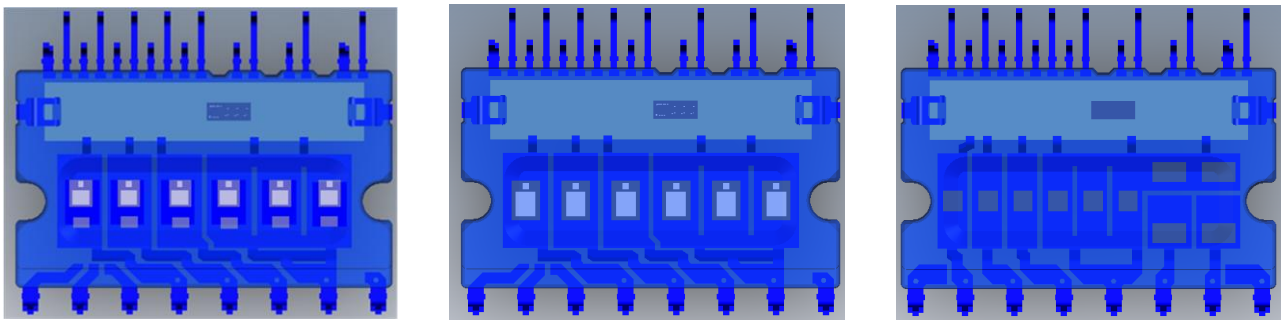


Figure 4. Package cross section of CIPOS™



(a) Inverter topology for IKCMxxx60xA

(b) Inverter topology for IGCMxxF60xA

(b) Inverter + Rectifier topology for IGCMxxB60xA

Figure 5. Flexible internal layout

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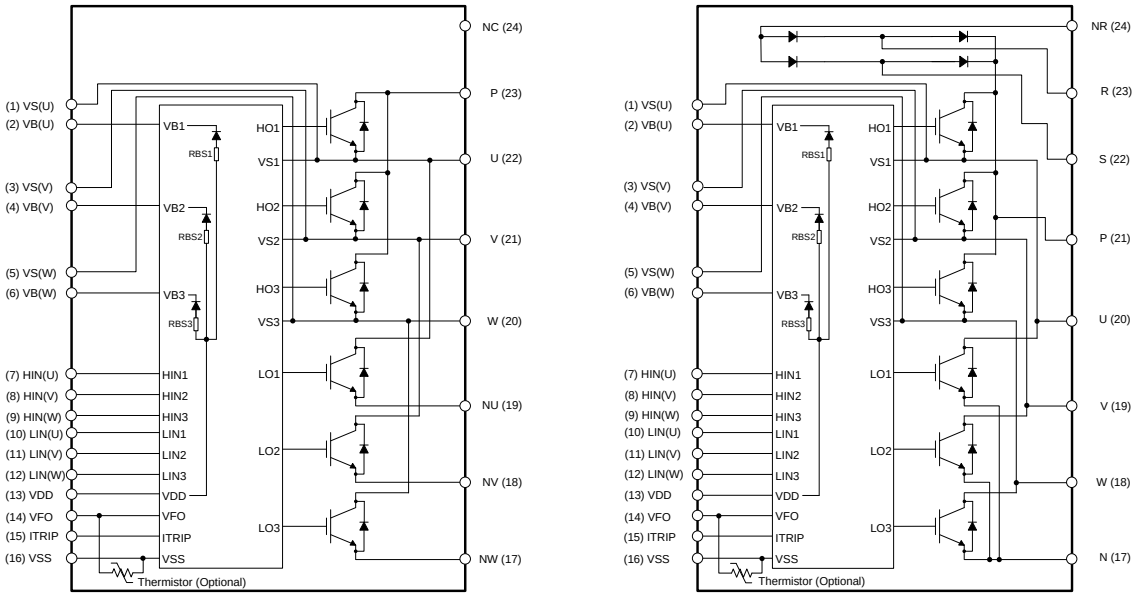
3 Product Synopsis

3.1 Internal circuit and features

Figure 6 illustrates the internal block diagram of the CIPOS™. It consists of a three-phase IGBT inverter circuit and a drive IC with control functions. The detailed features and integrated functions of CIPOS™ and the benefits acquired by using it are described as follows.



(a) Three phase bridge (b) Three phase bridge and rectifier bridge

Figure 6. Internal circuit

Features

- 600V/4A to 30A rating in one physical package size (mechanical layouts are identical)
- Single-phase input rectifier included for 6A products
- Fully isolated Dual In-Line (DIL) molded module
- Infineon reverse conducting IGBTs with monolithic body diode for IGCMxxF60xA
- Infineon Trench Stop IGBTs with separate body diode for IKCMxxx60xA
- Rugged SOI gate driver technology with stability against transient and negative voltage
- Integrated bootstrap functionality
- Matched delay times of all channels / Built in deadtime
- Over current shutdown
- Temperature sense
- Under-voltage lockout at all channels
- Low side emitter pins accessible for all phase current monitoring (open emitter)

- Cross-conduction prevention
- All 6 switches turn off during protection
- Active-high input signal logic
- Lead-free terminal plating; RoHS compliant
- No dummy pin

3.2 Electrical maximum ratings

Table 3. Detail description of absolute maximum ratings (IxCM10F60xA case)

Item	Symbol	Rating	Description
Max. blocking voltage	V_{CES}	600V	The sustained collector-emitter voltage of internal IGBTs.
Output current	I_C	±10A	The allowable AC continuous IGBT collector current at Tc=25°C.
Junction Temperature	T_J	-40 ~ 150°C	The maximum junction temperature rating considering temperature ripple of the power chips integrated within the CIPOS™ is 150°C.
Operating case temperature range	T_C	-40 ~ 100°C	Tc (case temperature) is defined to be the temperature just underneath the specified power chip. Please mount a temperature sensor in a heat-sink surface at the defined position in Figure 7 so as to get accurate temperature information.

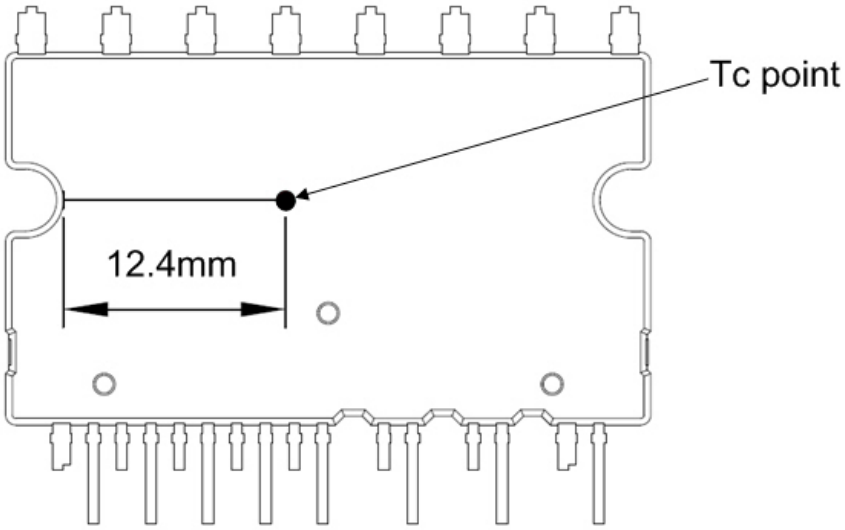


Figure 7. T_C measurement point

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3.3 Description of the input and output pins

Table 4 and Table 5 define the CIPOS^{TM} input and output pins. The detailed functional descriptions are as follows:

Table 4. Pin descriptions of CIPOS^{TM} for IxCMxxF60xA

Pin Number	Pin Name	Pin Description
1	VS(U)	U-phase high side floating IC supply offset voltage
2	VB(U)	U-phase high side floating IC supply voltage
3	VS(V)	V-phase high side floating IC supply offset voltage
4	VB(V)	V-phase high side floating IC supply voltage
5	VS(W)	W-phase high side floating IC supply offset voltage
6	VB(W)	W-phase high side floating IC supply voltage
7	HIN(U)	U-phase high side gate driver input
8	HIN(V)	V-phase high side gate driver input
9	HIN(W)	W-phase high side gate driver input
10	LIN(U)	U-phase low side gate driver input
11	LIN(V)	V-phase low side gate driver input
12	LIN(W)	W-phase low side gate driver input
13	VDD	Low side control supply
14	VFO	Fault output / temperature monitor
15	ITRIP	Over current shutdown input
16	VSS	Low side control negative supply
17	NW	W-phase low side emitter
18	NV	V-phase low side emitter
19	NU	U-phase low side emitter
20	W	Motor W-phase output
21	V	Motor V-phase output
22	U	Motor U-phase output
23	P	Positive bus input voltage
24	NC	No Connection

Table 5. Pin descriptions of CIPOS™ for IGCM06B60xA

Pin Number	Pin Name	Pin Description
1	VS(U)	U-phase high side floating IC supply offset voltage
2	VB(U)	U-phase high side floating IC supply voltage
3	VS(V)	V-phase high side floating IC supply offset voltage
4	VB(V)	V-phase high side floating IC supply voltage
5	VS(W)	W-phase high side floating IC supply offset voltage
6	VB(W)	W-phase high side floating IC supply voltage
7	HIN(U)	U-phase high side gate driver input
8	HIN(V)	V-phase high side gate driver input
9	HIN(W)	W-phase high side gate driver input
10	LIN(U)	U-phase low side gate driver input
11	LIN(V)	V-phase low side gate driver input
12	LIN(W)	W-phase low side gate driver input
13	VDD	Low side control supply
14	VFO	Fault output / temperature monitor
15	ITRIP	Over current shutdown input
16	VSS	Low side control negative supply
17	N	Low side common emitter
18	W	Motor W-phase output
19	V	Motor V-phase output
20	U	Motor U-phase output
21	P	Positive bus input voltage
22	R	Single phase diode bridge rectifier R input
23	S	Single phase diode bridge rectifier S input
24	NR	Negative bus voltage

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High side bias voltage pins for driving the IGBT

Pins : VB(U) – VS(U) , VB(V) – VS(V), VB(V) – VS(V)

- These pins provide the gate drive power to the high side IGBTs.
- The virtue of the ability to boot-strap the high side circuit scheme is that no external power supplies are required for the high side IGBTs
- Each boot-strap capacitor is charged from the VDD supply during the ON-state of the corresponding low side IGBT or the freewheeling state of the low side monolithic body diode.
- In order to prevent malfunctions caused by noise and ripple in supply voltage, a good quality (low ESR, low ESL) filter capacitor should be mounted very close to these pins

Low side bias voltage pin

Pin : VDD

- This is the control supply pin for the internal IC.
- In order to prevent malfunctions caused by noise and ripple in the supply voltage, a good quality (low ESR, low ESL) filter capacitor should be mounted very close to these pins.

Low side common supply ground pin

Pin : VSS

- This pin connects the control ground for the internal IC.

Signal input pins

Pin : HIN(U), HIN(V), HIN(W), LIN(U), LIN(V), LIN(W)

- These are pins to control the operation of the internal IGBTs .
- They are activated by voltage input signals. The terminals are internally connected to a schmitt trigger circuit composed of 5V-class CMOS.
- The signal logic of these pins is active-high. That is the IGBT associated with each of these pins will be turned "ON" when a sufficient logic voltage is applied to these pins.
- The wiring of each input should be as short as possible to protect the CIPOS^{TM} against noise influences.
- To prevent signal oscillations, an RC coupling is recommended as illustrated in Figure 9.

Over-current detection pins

Pin : ITRIP

- The current sensing shunt resistor should be connected between the pin ITRIP and the low side ground VSS to detect short-current (reference Figure 11). A RC filter should be connected to the pin ITRIP to eliminate noise.
- The integrated comparator is triggered, if the voltage V_{ITRIP} is higher than 0.47V. The shunt resistor should be selected to meet this level for the specific application. In case of a trigger event, the voltage at pin VFO is pulled down to LOW.
- The connection length between the shunt resistor and ITRIP pin should be minimized.

Fault output and temperature monitor pin

Pin : VFO

• This is the fault output alarm pin. An active low output is given on this pin for a fault state condition in the CIPOS^{TM}. The alarmed conditions are over-current detection or low side bias UV (Under Voltage) operation.

• The VFO output is of open drain configured. The VFO signal line should be pulled up to the logic power supply (5V / 3.3V) with proper resistance considering temperature monitor by parallel connected thermistor between VFO and VSS pins optionally.

Positive DC-link pin

Pin : P

• This is the DC-link positive power supply pin of the inverter.

• It is internally connected to the collectors of the high side IGBTs.

• In order to suppress the surge voltage caused by the DC-link wiring or PCB pattern inductance, connect a smoothing filter capacitor close to this pin. (Typically metal film capacitors are used)

Negative DC-link pins

Pin : NU, NV, NW

• These are the DC-link negative power supply pins (power ground) of the inverter.

• These pins are connected to the low side IGBT emitters of the each phase.

Inverter power output pin

Pin : U, V, W

• Inverter output pins for connecting to the inverter load (e. g. motor).

Single phase diode bridge rectifier input pins

Pin : R, S

• Rectifier input pins for connecting to the grid line.

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3.4 Outline drawings

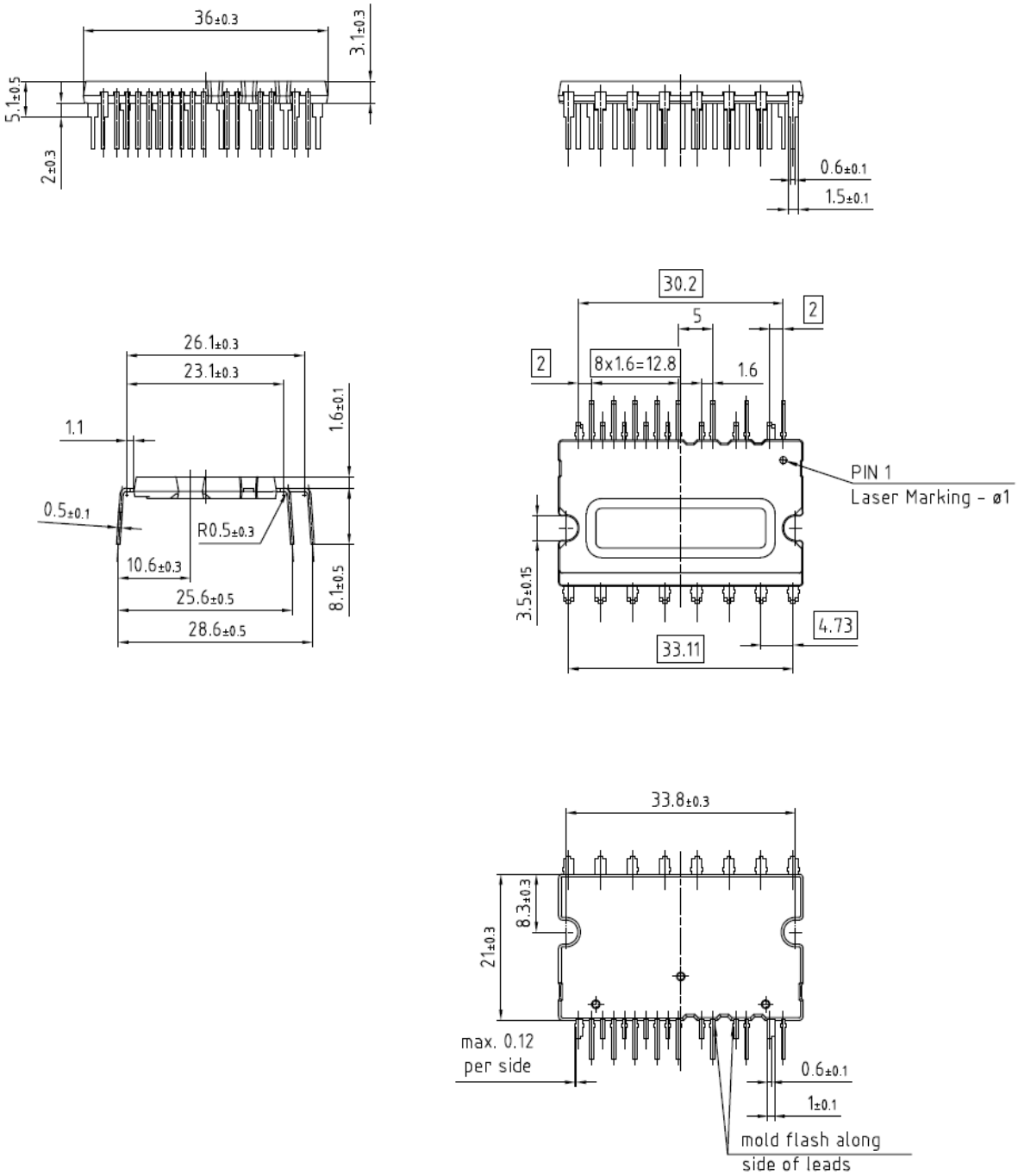

Figure 8. Package outline dimensions

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4 Interface Circuit and Layout Guide

4.1 Input/Output signal connection

Figure 9 shows the I/O interface circuit between micro controller and CIPOS™. Because the CIPOS™ input logic is active-high and there are internal pull-down resistors, external pull-down resistors are not needed. VFO output is open drain configured. This signal should be pulled up to the positive side of the 5V or 3.3V external logic power supply by a 3.6kΩ resistor considering a parallel connected thermistor between VFO and VSS pins.

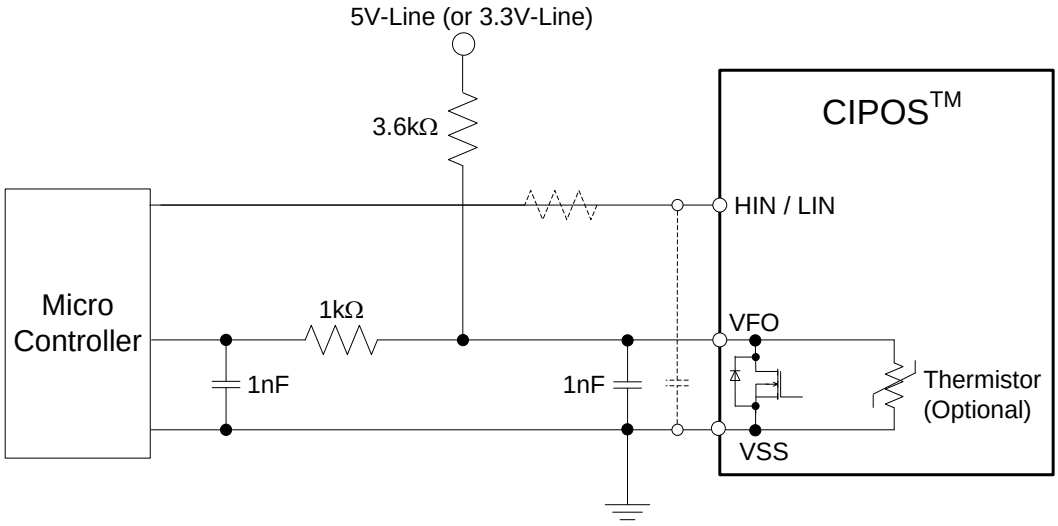

Figure 9. Recommended micro controller I/O interface circuit

Table 6. Maximum ratings of input and VFO pins

Item	Symbol	Condition	Rating	Unit
Module Supply Voltage	VDD	Applied between VDD – VSS	20	V
Input Voltage	VIN	Applied between HIN(U), HIN(V), HIN(W) – VSS LIN(U), LIN(V), LIN(W) – VSS	-1 ~ 10	V
Fault Output Supply Voltage	VFO	Applied between VFO – VSS	-0.5 ~ VDD+0.5	V

The input and fault output maximum rating voltages are shown in Table 6. Since the fault output is open drain configured and its rating is VDD+0.5V, 15V supply interface is possible. However, it is recommended that the fault output be configured with the 5V logic supply, which is the same as the input signals. It is also recommended that the by-pass capacitors be placed at both micro controller and CIPOS™ ends of the VFO, and signal line as close as possible to each device.

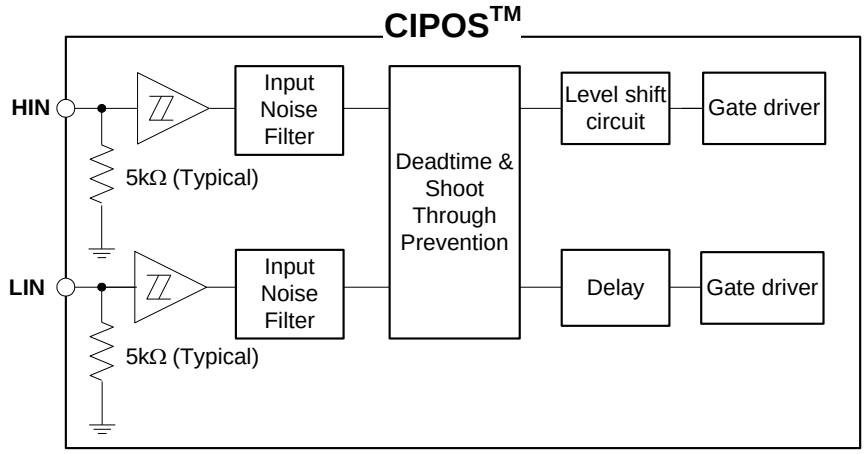

Figure 10. Internal structure of signal input terminals

Because CIPOS™ family employs active-high input logic, the sequence restriction between the control supply and the input signal during start-up or shut down operation comes to be removed. Therefore it makes the system fail-safe. In addition, pull-down resistors are built in to each input circuit. Thus, external pull-down resistors are not needed. This reduces the required external component count. Input Schmitt-trigger, noise filter and deadtime/shoot through prevention function provide beneficial noise rejection to short input pulses. Furthermore, by lowering the turn on and turn off threshold voltage of input signal as shown in Table 7, a direct connection to 3.3V-class micro controller or DSP is possible.

Table 7. Input threshold voltage ratings (at VDD = 15V, T_J = 25℃)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Logic "1" input voltage (LIN,HIN)	V_{IH}	HIN – VSS LIN – VSS	-	2.1	2.5	V
Logic "0" input voltage (LIN,HIN)	V_{IL}		0.7	0.9	-	V

As shown in Figure 10, the CIPOS™ input signal section integrates a 5kΩ (typical) pull-down resistor. Therefore, when using an external filtering resistor between the micro controller output and the CIPOS™ input attention should be given to the signal voltage drop at the CIPOS™ input terminals to satisfy the logic "1" input voltage requirement. For instance, R = 100Ω and C=1nF for the parts shown dotted in Figure 9.

4.2 General interface circuit example

Figure 11 and Figure 12 show typical application circuit for IxCMxxx60xA of interface schematic with control signals connected directly to a micro controller.

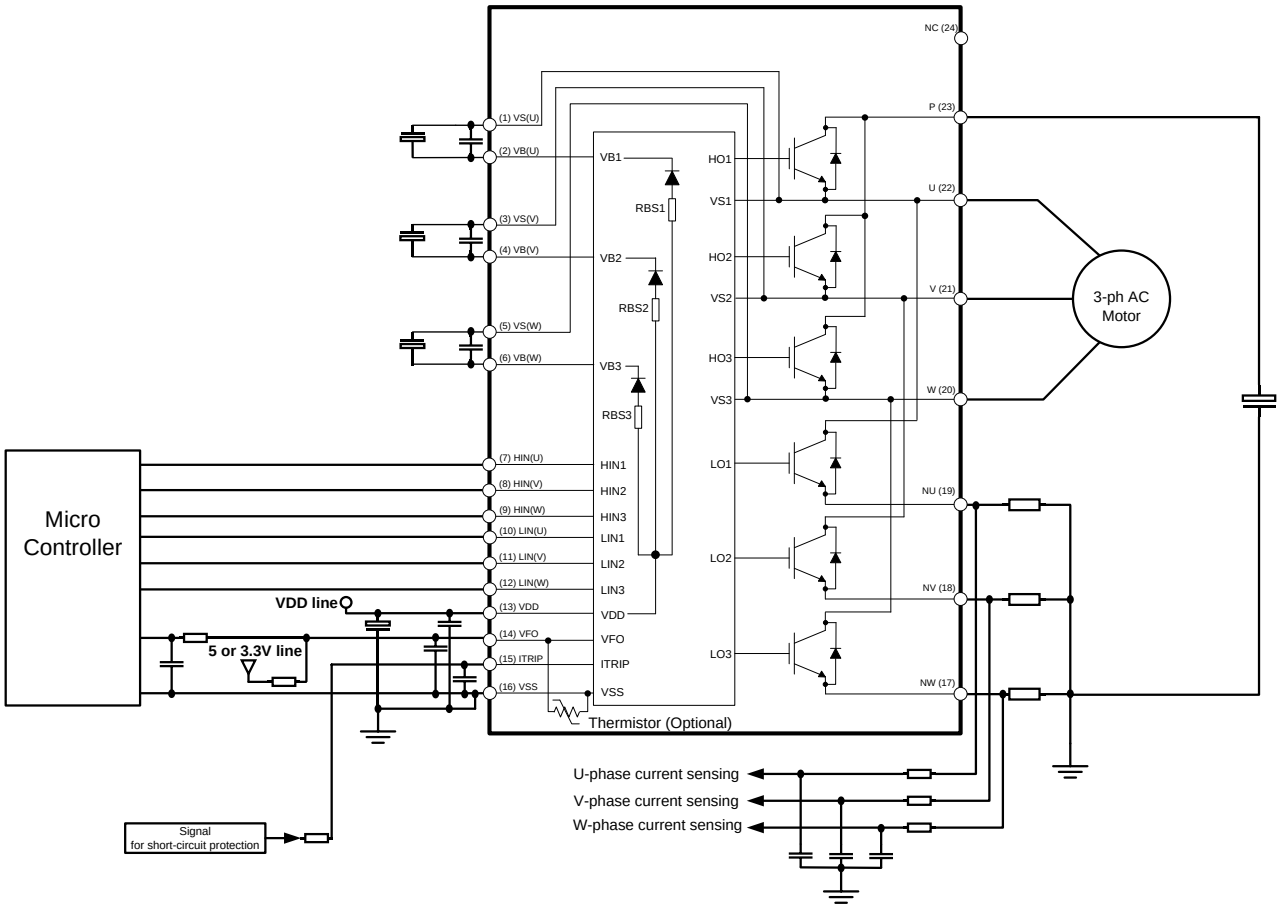

Figure 11. Example of application circuit for IxCMxxx60xA gives designators to the shunt filters and others which are mentioned in the text further on

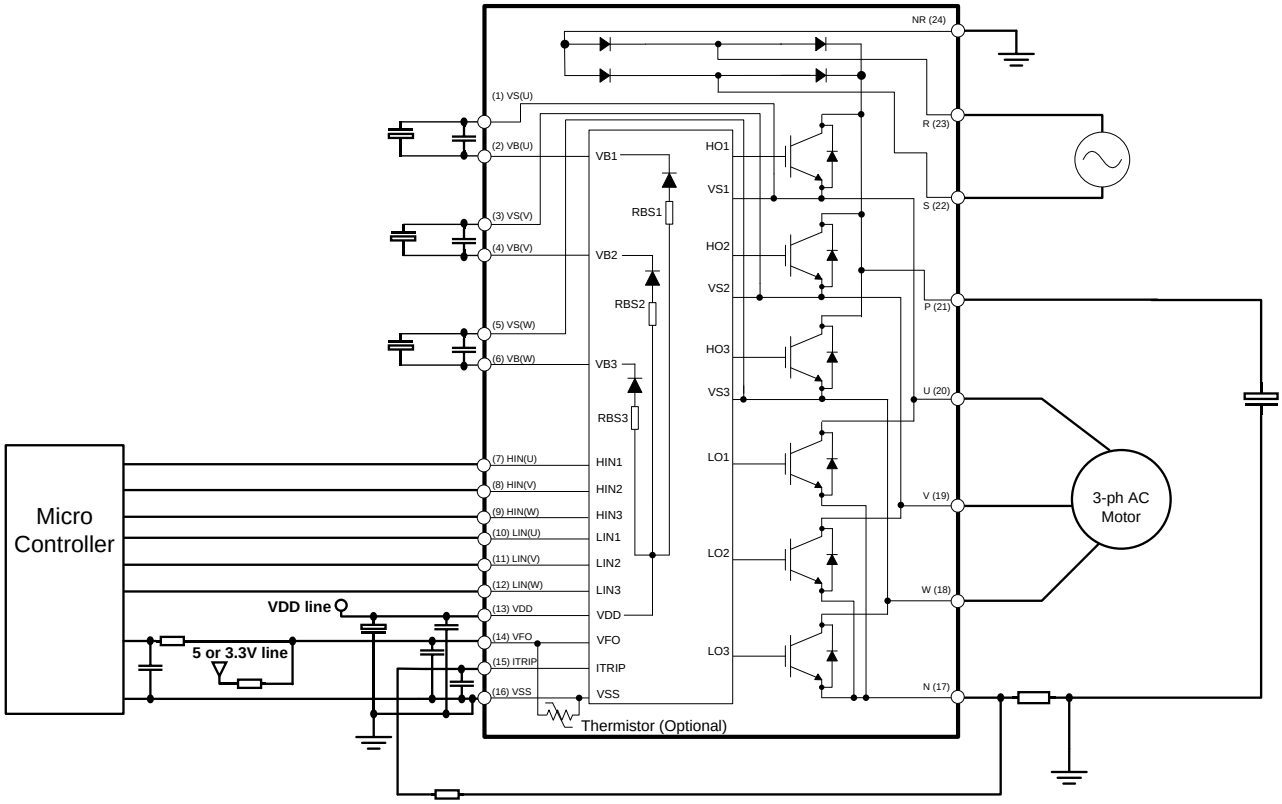

Figure 12. Example of application circuit for IGCM06B60xA gives designators to the shunt filters and others which are mentioned in the text further on

Notes:

1. The input signals are active-high configured. There is an internal 5kΩ pull-down resistor from each input signal line to VSS. When employing RC coupling circuits between micro controller and CIPOS^{TM}, the RC values are selected such that the input signals be compatible with the CIPOS^{TM} logic “1”/logic “0” input voltages.

2. To avoid malfunction, the wiring of each input should be as short as possible. (less than 2-3cm)

3. By virtue of integrating an application specific type IC inside CIPOS^{TM}, direct coupling to micro controller terminals without any opto-coupler or transformer isolation is possible.

4. VFO output is an open drain output. This signal line should be pulled up to the positive side of the 5V/3.3V logic power supply with a proper resistor R_{PU}. It is recommended that RC filter be placed at between CIPOS^{TM} and micro controller as close to the micro controller. (Please, refer to Figure 9)

5. To prevent protection function errors, the R_{ITRIP} and C_{ITRIP} wiring between ITRIP and N pins should be as short as possible. C_{ITRIP} wiring should be placed as close to VSS pin as possible.

6. The short-circuit protection time constant $\tau_{ITRIP} = R_{ITRIP} * C_{ITRIP}$ should be set in the range of 1~2μs. The overall short circuit reaction time of the control must ensure that the IGBT are turned off within 5μs.

7. Each capacitor should be mounted as close to the pins of the CIPOS^{TM} as possible.

8. Internal bootstrap resistance is around 40Ω. Especially, to reduce this resistance, external bootstrap circuitry is recommended. For more details, please refer to section 6.2.

9. VDD of 16V is recommended when only integrated bootstrap circuitry is used.

10. It is recommended that ground pin of micro-controller be directly connected to VSS pin.

4.3 Recommended the circuit current of power supply

Control and gate drive power for the CIPOS™ is normally provided by a single 15V supply that is connected to the module VDD and VSS terminal. The circuit current of VDD control supply of IGCM20F60xA is shown in below Table 8.

Table 8. The circuit current of control power supply of IGCM20F60xA (Unit:[mA])

Item		Static (Typ.)	Dynamic (Typ.)	Total (Typ.)
VDD=15V	FSW=5KHz	3.1	2.4	5.5
	FSW=15KHz	3.1	7.2	10.3
VDD=20V	FSW=20KHz	5.1	13.2	18.3

And, the circuit current of the 5V logic power supply (VFO & input terminals) is about 20mA.

Finally, the recommended minimum circuit currents of power supply are shown in Table 9 which is considered ripple current and enough margins at the worst conditions.

Table 9. The recommended minimum circuit current of power supply (Unit:[mA])

Item	The circuit current of +15V control supply	The circuit current of +5V logic supply
VDD ≤ 20V, FSW ≤ 20KHz	92	100

4.4 Recommended layout pattern for OCP & SCP function

It is recommended that ITRIP filter capacitor should be connected to pins of CIPOS^{TM} mini as short as possible. ITRIP filter capacitor should be connected to VSS pin directly without overlapped ground pattern. Signal ground and power ground should be as short as possible and connected at only one point via the filter capacitor of VDD line.

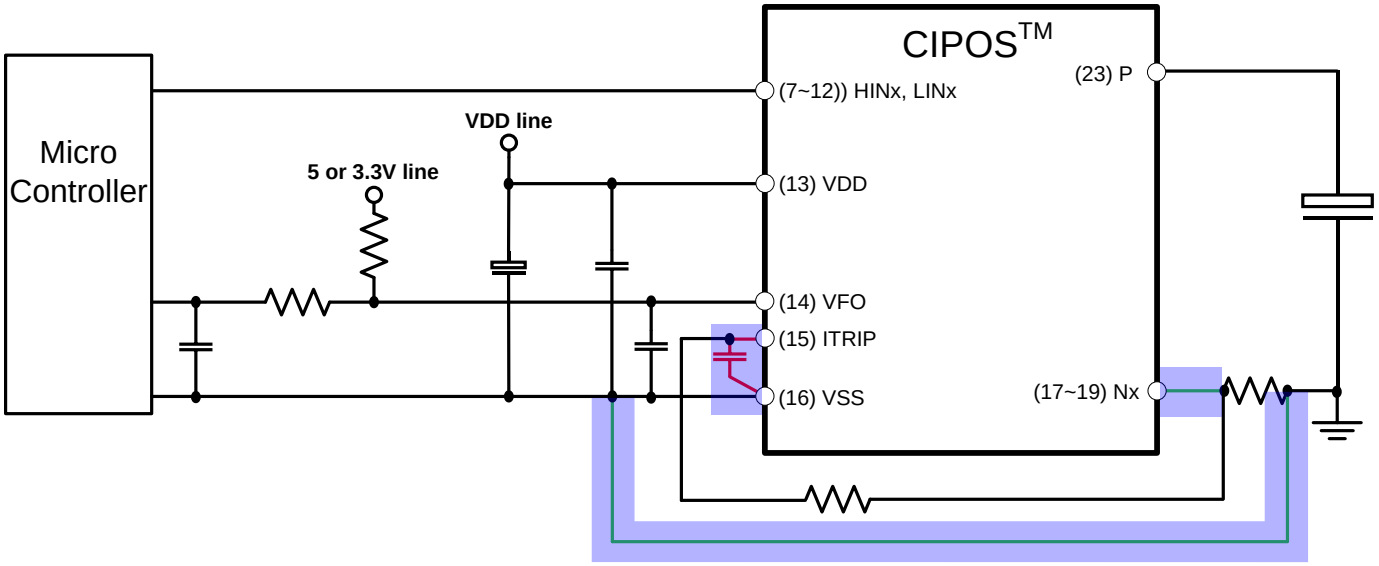

Figure 13. Recommended layout pattern for OCP & SCP function

4.5 Recommended wiring of shunt resistor and snubber capacitor

External current sensing resistors are applied to detect over current or phase currents. A long wiring pattern between the shunt resistors and CIPOS^{TM} will cause excessive surges that might damage the CIPOS^{TM}'s internal IC and current detection components, and this may also distort the sensing signals. To decrease the pattern inductance, the wiring between the shunt resistors and CIPOS^{TM} should be as short as possible.

As shown in the Figure 14, snubber capacitors should be installed in the right location so as to suppress surge voltages effectively. Generally a high frequency non-inductive capacitor of around 0.1 ~ 0.22μF is recommended. If the snubber capacitor is installed in the wrong location '1' as shown in Figure 14, the snubber capacitor cannot suppress the surge voltage effectively. If the capacitor is installed in the location '2', the charging and discharging currents generated by wiring inductance and the snubber capacitor will appear on the shunt resistor. This will impact the current sensing signal and the SC protection level will be a little lower than the calculated design value. The "2" position surge suppression effect is greater than the location '1' or '3'. The '3' position is a reasonable compromise with better suppression than in location '1' without impacting the current sensing signal accuracy. For this reason, the location '3' is generally used.

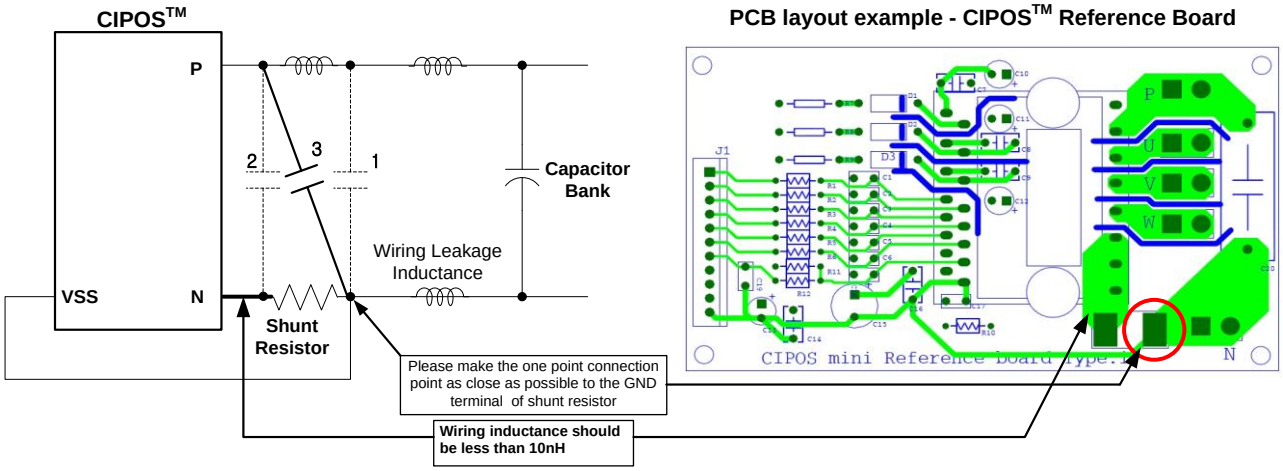

Figure 14. Recommended wiring of shunt resistor and snubber capacitor

4.6 Pin and screw holes coordinates for CIPOS™ footprint

Figure 15 shows CIPOS™ position on PCB to indicate center coordinates of each pin and screw hole in Table 10.

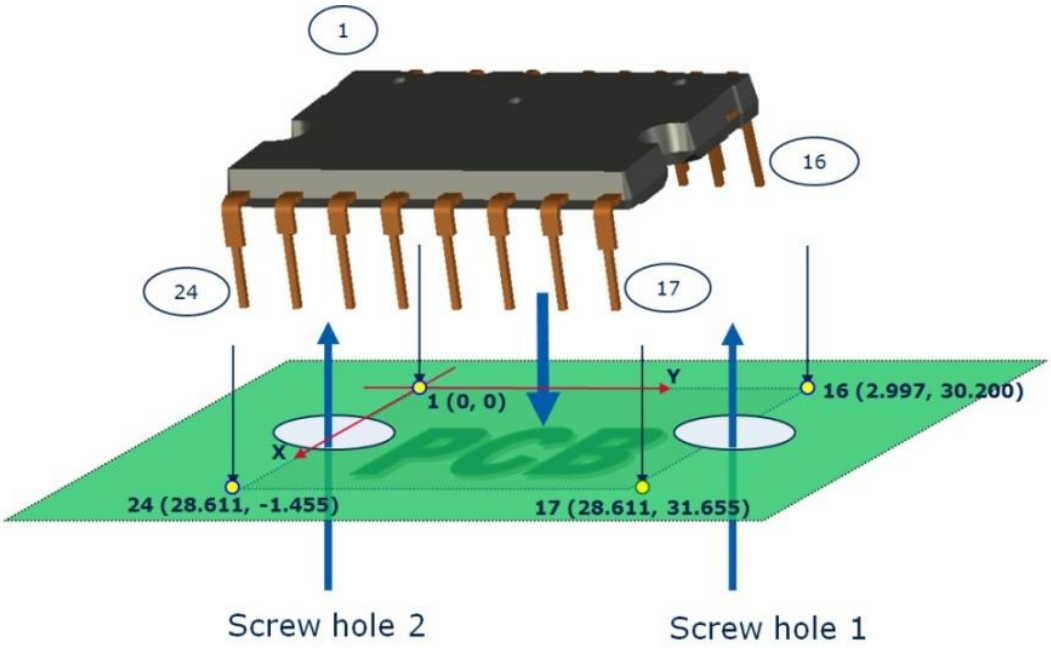

Figure 15. CIPOS™ position on PCB

Table 10. Pin & screw holes coordinates for CIPOS™ footprint (Unit:[mm])

Pin Number		X	Y	Pin Number		X	Y
Signal Pin	1	0.000	0.000	Signal Pin	14	2.997	26.600
	2	2.997	2.000		15	0.000	28.200
	3	0.000	5.400		16	2.997	30.200
	4	2.997	7.000	Power Pin	17	28.611	31.655
	5	0.000	10.400		18	28.611	26.925
	6	2.997	12.000		19	28.611	22.195
	7	0.000	15.400		20	28.611	17.465
	8	2.997	17.000		21	28.611	12.735
	9	0.000	18.600		22	28.611	8.005
	10	2.997	20.200		23	28.611	3.275
	11	0.000	21.800		24	28.611	-1.455
	12	2.997	23.400	Screw Hole	25	17.950	32.000
	13	0.000	25.000		26	17.950	-1.800

5 Protection Circuit

5.1 Under-voltage protection

Control and gate drive power for the CIPOS™ is normally provided by a single 15V supply that is connected to the module VDD and VSS terminals. For proper operation this voltage should be regulated to 15V ± 10%. Table 11 describes the behavior of the CIPOS™ for various control supply voltages. The control supply should be well filtered with a low impedance electrolytic capacitor and a high frequency decoupling capacitor connected right at the CIPOS™'s pins.

High frequency noise on the supply might cause the internal control IC to malfunction and generate erroneous fault signals. To avoid these problems, the maximum ripple on the supply should be less than ± 1V/µs.

The voltage at the module's VSS terminal is different from that at the N power terminal by the drop across the sensing resistor. It is very important that all control circuits and power supplies be referred to this point and not to the N terminal. If circuits are improperly connected, the additional current flowing through the sense resistor might cause improper operation of the short-circuit protection function. In general, it is best practice to make the common reference (VSS) a ground plane in the PCB layout.

The main control power supply is also connected to the bootstrap circuits that are used to establish the floating supplies for the high side gate drives.

When control supply voltage (V_{DD} and V_{BS}) falls down under UVLO (Under Voltage Lock Out) level, IGBT will turn off while ignoring the input signal.

Table 11. CIPOS™ functions versus control power supply voltage

Control Voltage Range [V]	CIPOS™ Function Operations
0 ~ 4	Control IC does not operate. Under voltage lockout and fault output does not operate.
4 ~ 13	As the under voltage lockout function is activated, control input signals are blocked and a fault signal VFO is generated.
13 ~ 14	IGBTs will be operated in accordance with the control gate input. Driving voltage is below the recommended range, so Vce(sat) and the switching loss will be larger than that under normal condition and high side IGBTs can't operate after V_{BS} initial charging because VBS can't reach to V_{BSUV+}.
14 ~ 18.5 for VDD **13.5 ~ 18.5 for VBS**	**Normal operation. This is the recommended operating condition.** **VDD of 16V is recommended when only integrated bootstrap circuitry is used. (14.5 ~ 18.5V VDD is recommended for IKCMxxx60xA)**
18.5 ~ 20 for VDD 18.5 ~ 20 for VBS	IGBTs are still operated. Because driving voltage is above the recommended range, IGBTs' switching is faster. It causes increasing system noise. And peak short circuit current might be too large for proper operation of the short circuit protection.
Over 20	Control circuit in the CIPOS™ might be damaged.

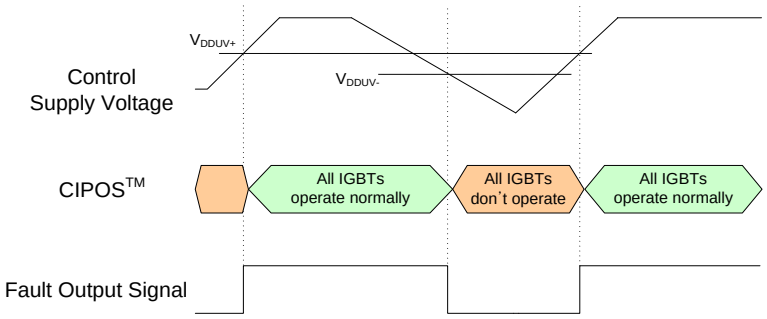

Figure 16. Timing chart of low side under-voltage protection function

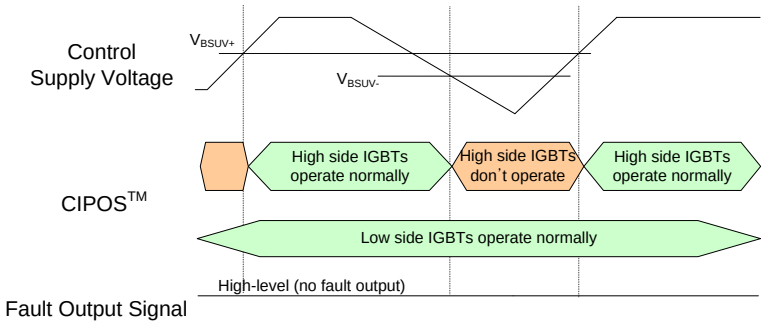

Figure 17. Timing chart of high side under-voltage protection function

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5.2 Over current protection

5.2.1 Timing chart of over current (OC) protection

The CIPOS™ has an over current shutdown function. Its internal IC monitors the voltage to the ITRIP pin and if this voltage exceeds the $V_{IT,TH+}$, which is specified in the devices datasheets, then a fault signal is activated and all IGBTs are turned off. Typically the maximum short circuit current magnitude is gate voltage dependant. A higher gate voltage results in a larger short circuit current. In order to avoid this potential problem, the maximum over current trip level is generally set to below 2 times the nominal rated collector current. The over current protection-timing chart is shown in Figure 18.

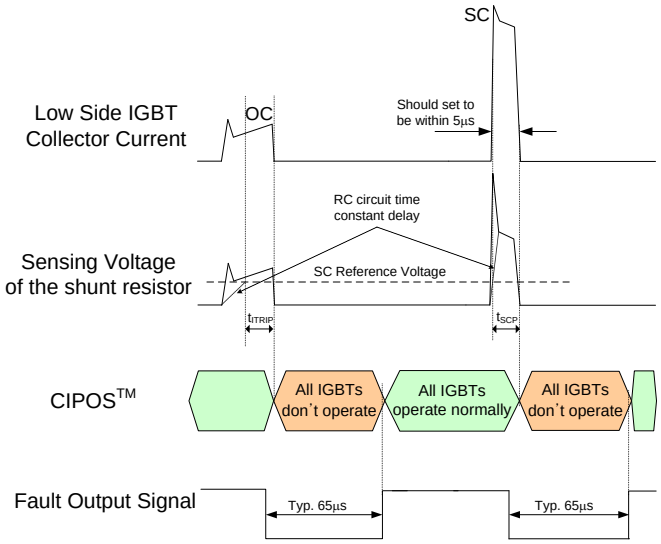


Figure 18. Timing chart of over current protection function

5.2.2 Selecting current sensing shunt resistor

The value of current sensing resistor is calculated by the following expression:

$$R_{SH} = \frac{V_{IT,TH+}}{I_{OC}} \quad (1)$$

Where $V_{IT,TH+}$ is the ITRIP positive going threshold voltage of CIPOS™ and typical 0.47V. I_{OC} is the current of OC detection level.

The maximum value of OC protection level should be set lower than the repetitive peak collector current in the datasheet considering the tolerance of shunt resistor.

For example, the maximum peak collector current of IGCM10F60xA is $18A_{peak}$, and thus, the recommended value of the shunt resistor is calculated as

$$R_{SH(min)} = \frac{0.47}{18} = 0.027\Omega$$

For the power rating of the shunt resistor, the below list should be considered:
- Maximum load current of inverter (Irms)
- Shunt resistor value at Tc=25°C (R_{SH})
- Power derating ratio of shunt resistor at T_{SH}=100°C according to the manufacturer´s datasheet
- Safety margin

And the power rating is calculated by following equation.

$$P_{SH} = \frac{I_{rms}^2 R_{SH} \times \text{margin}}{\text{Derating ratio}} \quad (2)$$

For example, in case of IGCM10F60xA and R_{SH}=27mΩ:
- Max. load current of inverter : $6A_{rms}$
- Power derating ratio of shunt resistor at T_{SH}=100°C : 80%
- Safety margin : 30%

$$P_{SH} = \frac{6^2 \times 0.027 \times 1.3}{0.8} = 1.58\text{W}$$

So the proper power rating of shunt resistor is over 2W.

Based on the previous equations, conditions, and calculation method, minimum shunt resistance and resistor power according to all kinds of CIPOS™ IGCMxxF60xA products are introduced as shown in Table 12.

It's noted that a proper resistance and over power than minimum value should be chosen considering over-current protection level required in the application set.

Table 12. Minimum R_{SH} and P_{SH}

Product	Maximum Peak Current	Minimum Shunt Resistance, R_{SH}	Minimum Shunt Resistor Power, P_{SH}
IKCM30F60xA	60	8mΩ	5W
IGCM20F60xA	45	11mΩ	4W
IGCM15F60xA	30	16mΩ	3W
IGCM10F60xA	18	27mΩ	2W
IGCM06x60xA	12	40mΩ	1W
IGCM04F60xA	8	60mΩ	0.7W
IKCM10H60xA	16	30mΩ	2W
IKCM15H60xA	24	20mΩ	3.5W
IKCM20H60xA	34	14mΩ	5W

5.2.3 Delay time

The RC filter is necessary in the over current sensing circuit to prevent malfunction of OC protection caused by noise. The RC time constant is determined by applying time of noise and the withstand time capability of IGBT.

When the sensing voltage on shunt resistor exceeds ITRIP positive going threshold ($V_{IT,TH+}$), this voltage is applied to the ITRIP pin of CIPOS^{TM} via the RC filter. Table 13 shows the specification of the OC protection reference level. The filter delay time (t_{FILTER}) that the input voltage of ITRIP pin rises to the ITRIP positive threshold voltage is caused by RC filter time constant.

In addition there is the shutdown propagation delay of Itrip (t_{ITRIP}). Please refer to the Table 14.

Table 13. Specification of OC protection reference level ' $V_{IT,TH+}$'

Item	Min.	Typ.	Max.	Unit
ITRIP positive going threshold $V_{IT,TH+}$	0.40	0.47	0.54	V

Table 14. Internal delay time of OC protection circuit

Item		Condition	Min.	Typ.	Max.	Unit
Shut down propagation delay (t_{ITRIP})	IKCM30F60xA	I_{out} =20A, from $V_{IT,TH+}$to 10% I_{out}	-	1420	-	ns
	IGCM20F60xA	I_{out} =15A, from $V_{IT,TH+}$to 10% I_{out}	-	1540	-	
	IGCM15F60xA	I_{out} =10A, from $V_{IT,TH+}$to 10% I_{out}	-	1340	-	
	IGCM10F60xA	I_{out} =6A, from $V_{IT,TH+}$to 10% I_{out}	-	1260	-	
	IGCM06x60xA	I_{out} =4A, from $V_{IT,TH+}$to 10% I_{out}	-	1300	-	
	IGCM04F60xA	I_{out} =2.5A, from $V_{IT,TH+}$to 10% I_{out}		1320		
	IKCM10H60xA	I_{out} =6A, from $V_{IT,TH+}$to 10% I_{out}	-	1250	-	
	IKCM15H60xA	I_{out} =10A, from $V_{IT,TH+}$to 10% I_{out}	-	1300	-	
	IKCM20H60xA	I_{out} =15A, from $V_{IT,TH+}$to 10% I_{out}	-	1300	-	

Therefore the total time from ITRIP positive going threshold ($V_{IT,TH+}$) to the shut down of the IGBT becomes:

$$t_{TOTAL} = t_{FILTER} + t_{ITRIP} \quad (3)$$

Shut down propagation delay is in inverse proportion to the current range, therefore t_{ITRIP} is reduced at higher current condition than condition of table 14. The total delay must be less than 5μs of short circuit withstand time (t_{SC}) in datasheet. Thus, RC time constant should be set in the range of 1~2μs. It is recommended that R of 1.8kΩ and C of 1nF.

5.3 Fault output circuit

Table 15. Fault-output maximum ratings

Item	Symbol	Condition	Rating	Unit
Fault Output Supply Voltage	V_{FO}	Applied between VFO-VSS	-0.5~ V_{DD}+0.5	V
Fault Output Current	I_{FO}	Sink current at VFO pin	10	mA

Table 16. Electric characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Fault Output Supply Voltage	I_{FO}	V_{ITRIP} = 0V, V_{FO}=5V	-	2	-	nA
	V_{FO}	I_{FO} = 10mA, V_{ITRIP}=1V	-	0.5	-	V

Because VFO terminal is an open drain type, it must be pulled up to the high level via a pull-up resistor. The resistor has to satisfy the above specifications.

5.4 Over temperature protection

CIPOS™ with optional temperature sensing function have one pin for both fault-output and temperature sensing. Figure 19 shows internal thermistor resistance characteristics according to thermistor temperature. For over temperature protection, a circuitry is introduced in this section. As shown in Figure 20, VFO pin is connected directly to ADC and fault detection terminals of micro controller. This circuit is very simple and IGBTs have to be shut down by micro controller. For example, when R1 is 3.6kΩ, then VFO at about 100°C of thermistor temperature is 2.95$V_{typ.}$at Vctr=5V and 1.95V at Vctr=3.3V, as shown in Figure 21. It's noted that VFO for over temperature protection should be not less than micro controller fault trip level.

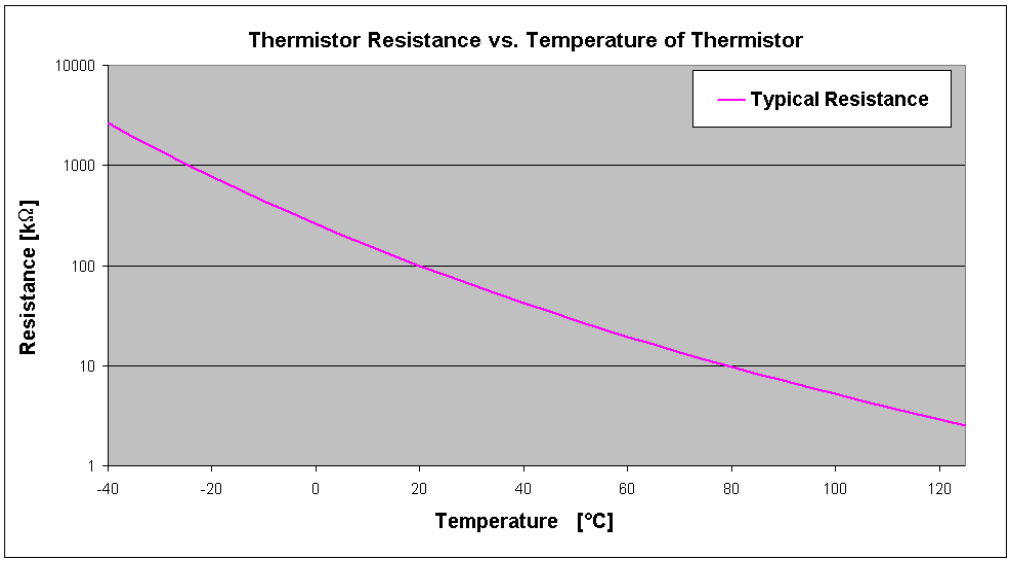


Figure 19. Internal thermistor resistance characteristics according to thermistor temperature

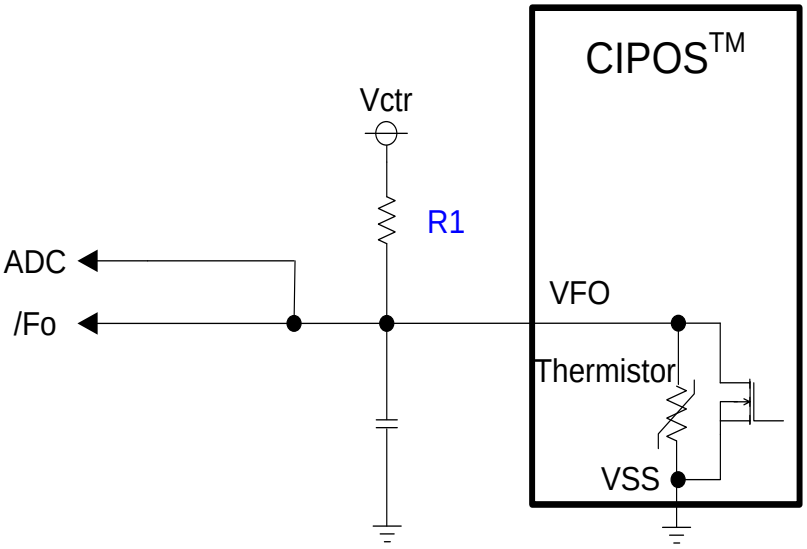


Figure 20. Circuit proposals for over temperature protection

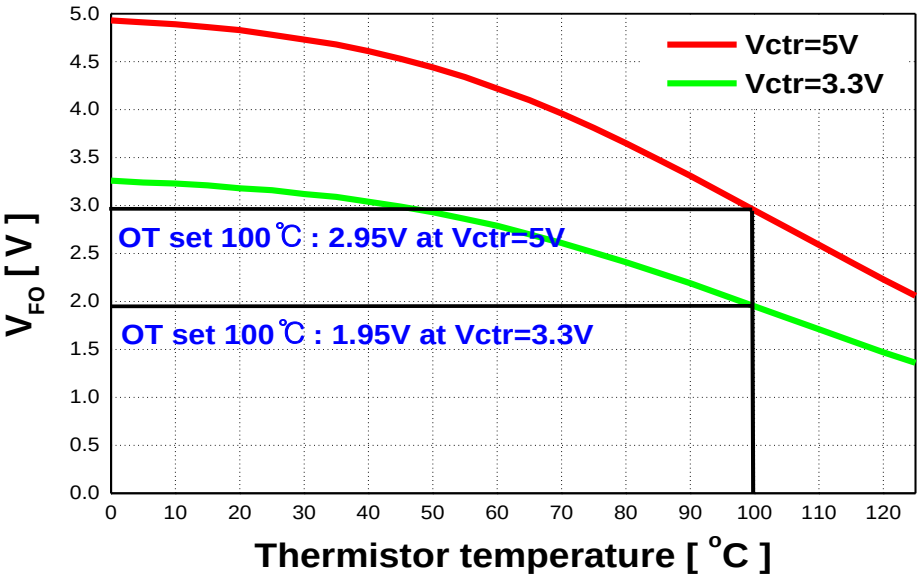


Figure 21. Voltage of VFO pin according to thermistor temperature

6 Bootstrap Circuit

6.1 Operation of bootstrap circuit

The V_{BS} voltage, which is the voltage difference between $V_{B\,(U,\,V,\,W)}$ and $V_{S\,(U,\,V,\,W)}$, provides the supply to the IC within the CIPOS™. This supply must be in the range of 13.0~18.5V to ensure that the IC can fully drive

the high side IGBT. The CIPOS^{TM} includes an under-voltage detection function for the V_{BS} to ensure that the IC does not drive the high side IGBT, if the V_{BS} voltage drops below a specified voltage (refer to the datasheet). This function prevents the IGBT from operating in a high dissipation mode. Please note here, that the under voltage lockout function of any high side section acts only on the triggered channel without any feedback to the control level.

There are a number of ways in which the V_{BS} floating supply can be generated. One of them is the bootstrap method described here. This method has the advantage of being simple and cheap. However, the duty cycle and on-time are limited by the requirement to refresh the charge in the bootstrap capacitor. The bootstrap supply is formed by a combination of an external diode, resistor and capacitor as shown in Figure 23. The current flow path of the bootstrap circuit is shown in Figure 22. When V_S is pulled down to ground (either through the low side or the load), the bootstrap capacitor (C_{BS}) is charged through the bootstrap diode (D_{BS}) and the resistor (R_{BS}) from the V_{DD} supply.

6.2 Internal bootstrap functionality characteristics

CIPOS^{TM} includes three bootstrap functionalities in internal drive IC, which consist of three diodes and three resistors, as shown in Figure 6. Typical value of internal bootstrap resistor is 40Ω at room temperature. For more information, please refer to the Table 17. It's noted that R_{BS2} and R_{BS3} have same value to R_{BS1}.

VDD of 16V is recommended when only integrated bootstrap circuitry is used.

Table 17. Electrical characteristics of internal bootstrap parameters

Description	Condition	Symbol	Min.	Typ.	Max.	Unit
Repetitive peak reverse voltage		V_{RRM}	600			V
Bootstrap resistance of U-phase	VS2 or VS3=300V, T_J=25°C VS2 and VS3=0V, T_J=25°C VS2 or VS3=300V, T_J=125°C VS2 and VS3=0V, T_J=125°C	R_{BS1}		35 40 50 65		Ω
Reverse recovery	I_F=0.6A, di/dt=80A/μs	t_{rr_BS}		50		ns
Forward voltage drop	I_F=20mA, VS2 and VS3=0V	V_{F_BS}		2.6		V

High voltage supply to gate driver between VSx and VSS is limited to dynamic operation.

If it is necessary to reduce integrated bootstrap resistance, external bootstrap circuitry is recommended. For example, when 39Ω of bootstrap resistor and 1N4937 of bootstrap diode are connected externally to CIPOS^{TM}, bootstrap resistance becomes around 25Ω, as shown in Table 18.

Table 18. Bootstrap resistance with external bootstrap circuitry (39Ω and 1N4937)

Description	Condition	Symbol	Min.	Typ.	Max.	Unit
Bootstrap resistance of U-phase	T_J=25°C T_J=125°C	R_{BS1}		24 28		Ω

6.3 Initial charging of bootstrap capacitor

An adequate on-time duration of the low side IGBT to fully charge the bootstrap capacitor is required for initial bootstrap charging. The initial charging time (t_{charge}) can be calculated from the following equation:

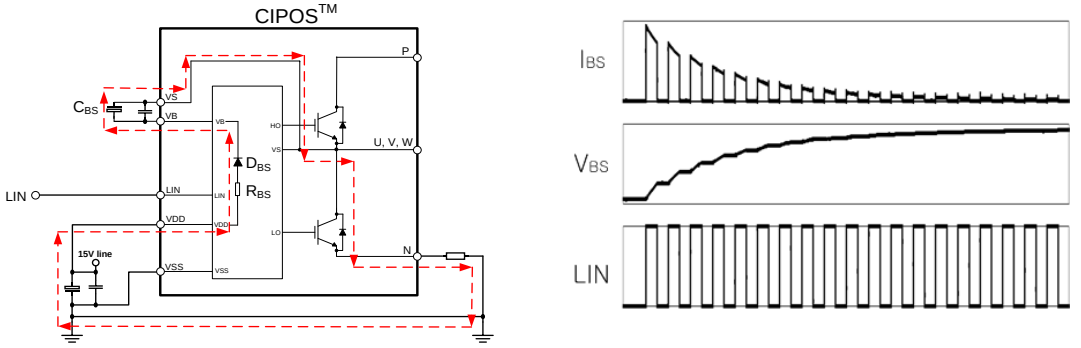
$$t_{charge} \geq C_{BS} \times R_{BS} \times \frac{1}{\delta} \times \ln\left(\frac{V_{DD}}{V_{DD} - V_{BS(min)} - V_{FD} - V_{LS}}\right) \quad (4)$$

V_{FD} = Forward voltage drop across the bootstrap diode

$V_{BS(min)}$ = The minimum value of the bootstrap capacitor

V_{LS} = Voltage drop across the low side IGBT

δ = Duty ratio of PWM



(a) Bootstrap circuit (b) Timing chart of initial bootstrap charging

Figure 22. Bootstrap circuit operation and initial charging

6.4 Selection of a bootstrap capacitor

The bootstrap capacitance can be calculated by:

$$C_{BS} = \frac{I_{leak} \times \Delta t}{\Delta V} \quad (5)$$

Where Δt = maximum ON pulse width of high side IGBT

ΔV = the allowable discharge voltage of the C_{BS}.

I_{leak}= maximum discharge current of the C_{BS} mainly via the following mechanisms:

- Gate charge for turning the high side IGBT on
- Quiescent current to the high side circuit in the IC
- Level-shift charge required by level-shifters in the IC
- Leakage current in the bootstrap diode
- C_{BS} capacitor leakage current (ignored for non-electrolytic capacitors)
- Bootstrap diode reverse recovery charge

Practically, a leakage current of 1mA is recommended as a calculation basis for CIPOS™. By taking consideration of dispersion and reliability, the capacitance is generally selected to be 2~3 times of the calculated one. The C_{BS} is only charged when the high side IGBT is off and the VS voltage is pulled down to ground. Therefore, the on-time of the low side IGBT must be sufficient to ensure that the charge drawn from

the C_{BS} capacitor can be fully replenished. Hence, inherently there is a minimum on-time of the low side IGBT (or off-time of the high side IGBT).

The bootstrap capacitor should always be placed as close to the pins of the CIPOS™ as possible. At least one low ESR capacitor should be used to provide good local de-coupling. For example, a separate ceramic capacitor close to the CIPOS™ is essential, if an electrolytic capacitor is used for the bootstrap capacitor. If the bootstrap capacitor is either a ceramic or tantalum type, it should be adequate for local decoupling.

6.5 Charging and discharging of the bootstrap capacitor during PWM-inverter operation

The bootstrap capacitor C_{BS} charges through the bootstrap diode D_{BS} and resistor R_{BS} according to Figure 22 from the V_{DD} supply when the high side IGBT is off, and the V_S voltage is pulled down to ground. It discharges when the high side IGBT or diode are on.

Example 1: Selection of the initial charging time

An example of the calculation of the minimum value of the initial charging time is given with reference to equation (4).

Conditions:

C_{BS} = 4.7µF, R_{BS} = 40Ω, Duty Ratio (δ)= 0.5, D_{BS} =Internal bootstrap diode, V_{DD} = 15V, V_{FD} = 0.9V

$V_{BS\,(min)}$ = 13.5V, V_{LS} = 0.1V

$$t_{charge} \geq 4.7\mu F \times 40\Omega \times \frac{1}{0.5} \times \ln\left(\frac{15V}{15V - 13.5V - 0.9V - 0.1V}\right) \cong 1.1ms$$

In order to ensure safety, it is recommended that the charging time must be at least three times longer than the calculated value.

Example 2: The minimum value of the bootstrap capacitor

Conditions:

ΔV=0.1V, I_{leak}=1mA

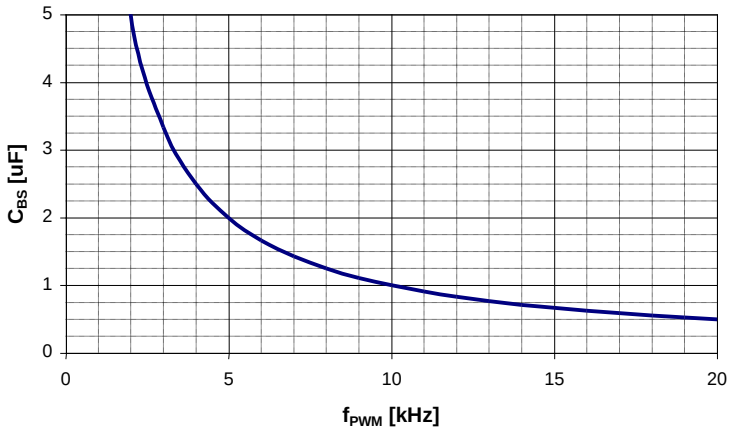


Figure 23. Bootstrap capacitance as a function of the switching frequency

Figure 23 shows the curve corresponding to equation (5) for a continuous sinusoidal modulation, if the voltage ripple ΔV_{BS} is 0.1V. The recommended bootstrap capacitance for a continuous sinusoidal modulation method is therefore in the range up to 4.7µF for most switching frequencies. In other PWM method case like a discontinuous sinusoidal modulation, tp must be set the longest period of the low side IGBT off.

Note that this result is only an example. It is recommended that the system design considers of the actual control pattern and lifetime of components.

7 Thermal System Design

7.1 Introduction

The thermal design of a system is a key issue of CIPOS™ included electronic systems such as drives. In order to avoid overheating and / or to increase the reliability, two design criteria are of importance:

- Low power losses
- Low thermal resistance from junction to ambient

The first criterion is already fulfilled when choosing CIPOS™ as intelligent power module for your application. To get the most out of your system a proper heat sink choice is necessary. A good thermal design either allows to maximize the power or to increase the reliability of the system (by reducing the maximum temperature). This application note will give a short introduction to power losses, heat sinks, helping to understand the mode of operation and to find the right heat sink for a specific application.

For the thermal design one needs:

- The maximum power losses $P_{sw,i}$ of each power switch.
- The maximum junction temperature $T_{J,max}$ of the power semiconductors.
- The junction to ambient thermal resistance impedance $Z_{th,J-A}$. For stationary considerations the static thermal resistance $R_{th,J-A}$ is sufficient. This thermal resistance comprises the junction to case thermal resistance $R_{th,J-C}$ as provided in datasheets, the case to heat sink thermal resistance $R_{th,C-HS}$ accounting for the heat flow through the thermal interface material between heat sink and the power module and the heatsink to ambient thermal resistance $R_{th,HS-A}$. Each thermal resistance can be extended to it's corresponding thermal impedance by adding the thermal capacitances.
- The maximum allowable ambient temperature $T_{A,max}$.

Furthermore all heat flow paths need to be identified. Figure 24 presents a typical simplified equivalent circuit for the thermal network. This circuit is simplified as it omits thermal capacitances and typically negligible heat paths such as the heat transfer from the module surface directly to the ambient via convection and radiation.

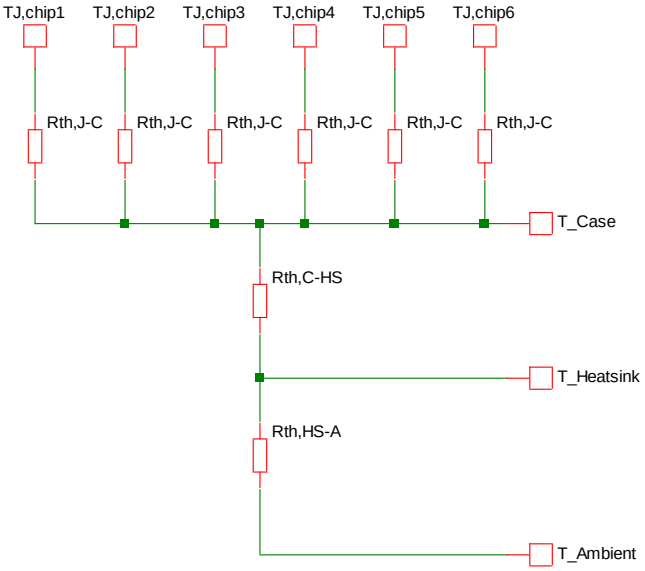


Figure 24. Simplified thermal equivalent circuit

7.2 Power loss

The total power losses in the CIPOS™ are composed of conduction and switching losses in the IGBTs. The loss during the turn-off steady state can be ignored because it is very small amount and has little effect on increasing the temperature in the device. The conduction loss depends on the dc electrical characteristics of the device i.e. saturation voltage. Therefore, it is a function of the conduction current and the device's junction temperature. On the other hand the switching loss is determined by the dynamic characteristics like turn-on/off time and over-voltage/current. Hence, in order to obtain the accurate switching loss, we should consider the DC-link voltage of the system, the applied switching frequency and the power circuit layout in addition to the current and temperature.

In this chapter, based on a PWM-inverter system for motor control applications, detailed equations are shown to calculate both losses of the CIPOS™. They are for the case that 3-phase continuous sinusoidal PWM is adopted. For other cases like 3-phase discontinuous PWMs, please refer to [4].

7.2.1 Conduction loss

The typical characteristics of forward drop voltage are approximated by the following linear equation for the IGBT and the diode, respectively.

$$V_{IGBT} = V_I + R_I \cdot i$$
$$V_{DIODE} = V_D + R_D \cdot i \quad (6)$$

V_I = Threshold voltage of IGBT V_D = Threshold voltage of monolithic body diode

R_I = on-state slope resistance of IGBT R_D = on-state slope resistance of monolithic body diode

Assuming that the switching frequency is high, the output current of the PWM-inverter can be assumed to be sinusoidal. That is,

$$i = I_{peak}\cos(\theta - \varphi) \tag{7}$$

Where φ is the phase-angle difference between output voltage and current. Using equations (6) and (7), the conduction loss of one IGBT and its monolithic body diode can be obtained as follows.

$$P_{con.I} = \frac{1}{2\pi}\int_0^{\pi} \xi(V_{IGBT} \times i)d\theta = \frac{I_{peak}}{2\pi}V_I + \frac{I_{peak}}{8}V_I MI\cos\varphi + \frac{I_{peak}^{\ 2}}{8}R_I + \frac{I_{peak}^{\ 2}}{3\pi}R_I MI\cos\varphi \tag{8}$$

$$P_{con.D} = \frac{1}{2\pi}\int_0^{\pi} (1-\xi)(V_{DIODE} \times i)d\theta = \frac{I_{peak}}{2\pi}V_D - \frac{I_{peak}}{8}V_D MI\cos\varphi + \frac{I_{peak}^{\ 2}}{8}R_D - \frac{I_{peak}^{\ 2}}{3\pi}R_D MI\cos\varphi \tag{9}$$

$$P_{con} = P_{con.I} + P_{con.D} \tag{10}$$

Where ξ is the duty cycle in the given PWM method.

$$\xi = \frac{1 + MI\cos\theta}{2} \tag{11}$$

Where MI is the PWM modulation index (MI, defined as the peak phase voltage divided by the half of dc link voltage).

It should be noted that the total inverter conduction losses are six times of the P_{con}.

7.2.2 Switching loss

Different devices have different switching characteristics and they also vary according to the handled voltage/current and the operating temperature/frequency. However, the turn-on/off loss energy (Joule) can be experimentally measured indirectly by multiplying the current and voltage and integrating over time, under a given circumstance. Therefore the linear dependency of a switching energy loss on the switched-current is expressed during one switching period as follows.

$$Swtitching \quad energy \quad loss = (E_I + E_D) \times i \quad [joule] \tag{12}$$

$$E_I = E_{I.ON} + E_{I.OFF} \tag{13}$$

$$E_D = E_{D.ON} + E_{D.OFF} \tag{14}$$

Where, E_I i is the switching loss energy of the IGBT and E_D i is for its monolithic body diode. E_I and E_D can be considered a constant approximately.

As mentioned in the equation (7), the output current can be considered a sinusoidal waveform and the switching loss occurs every PWM period in the continuous PWM schemes. Therefore, depending on the switching frequency of f_{SW}, the switching loss of one device is the following equation (15).

$$P_{sw} = \frac{1}{2\pi}\int_0^{\pi} (E_I + E_D)\ i\ f_{sw}d\varphi = \frac{(E_I + E_D)f_{sw}I_{peak}}{\pi} \tag{15}$$

Where E_I is a unique constant of IGBT related to the switching energy and different IGBT has different E_I value. E_D is one for diode. Those should be derived by experimental measurement. From the equation (15), it should be noted that the switching losses are a linear function of current and directly proportional to the switching frequency.

7.3 Thermal impedance

In practical operation, the power loss P_D is cyclic and therefore the transient impedance needs to be considered. The thermal impedance is typically represented by a RC equivalent circuit as shown in Figure 25. For pulsed power loss, the thermal capacitance effect delays the rise in junction temperature, and thus permits a heavier loading of the CIPOS™. Figure 26 shows thermal impedance from junction to case curves of IGCM10F60xA. The thermal resistance goes into saturation in about 10 seconds. Other kinds of CIPOS™ also show similar characteristics.

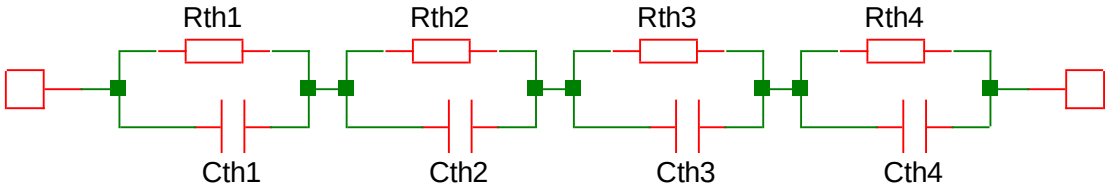


Figure 25. Thermal impedance RC equivalent circuit

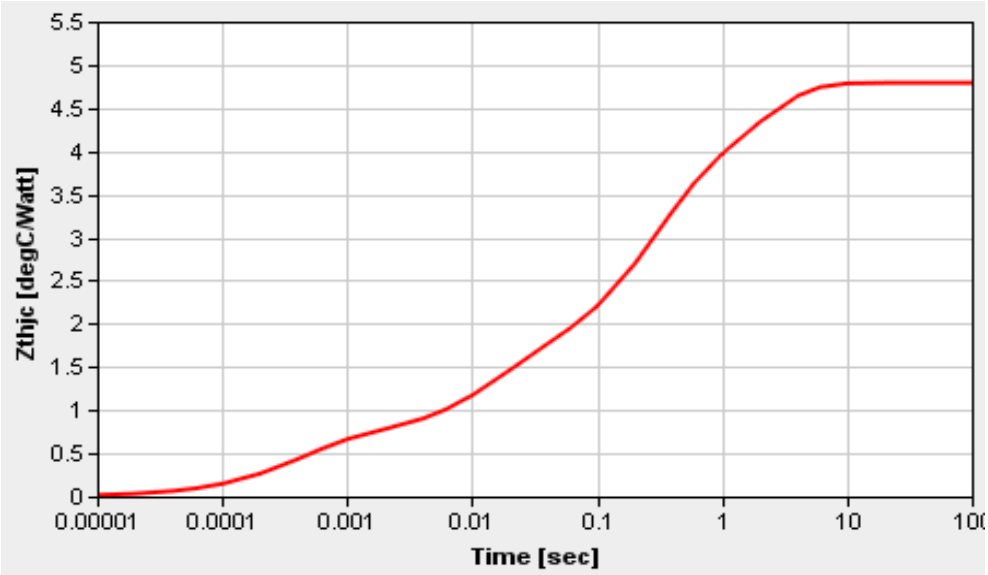


Figure 26. Thermal impedance curves (IGCM10F60xA)

7.4 Temperature rise considerations and calculation example

The simulator CIPOSIM allows calculating power losses and temperature profiles for a constant case temperature. The result of loss calculation using the typical characteristics is shown in Figure 27 as “Effective current versus carrier frequency characteristics” (for VPN=300V, VDD=15V, VCE(sat)=typical, Switching loss=typical, Tj=150°C, Tc=100°C, Rth(j-c) = Max., P.F=0.8, 3-phase continuous PWM modulation, 60Hz sine waveform output).

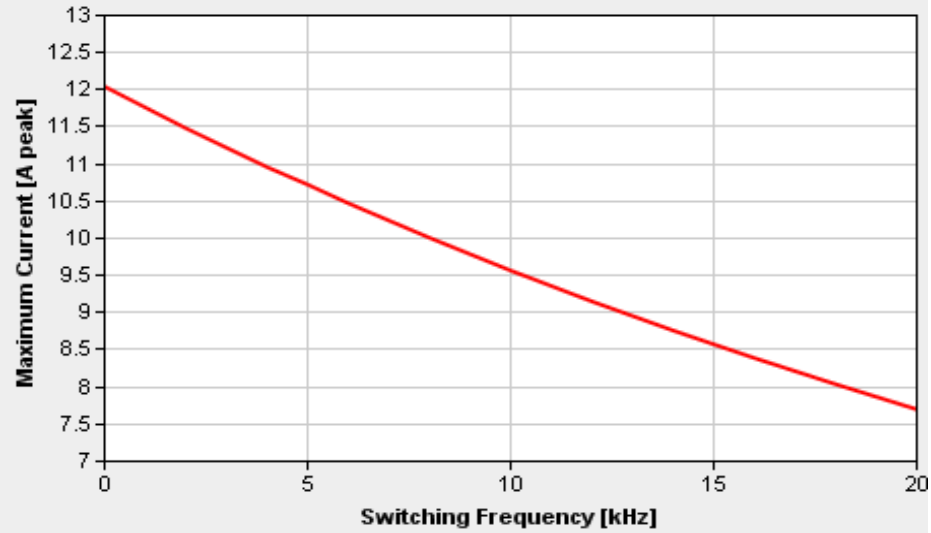


Figure 27. Effective current – carrier frequency characteristics of IGCM10F60xA [5]

Figure 27 shows an example of an inverter operated under the condition of Tc=100°C. It indicates the effective current I_o which can be output when the junction temperature Tj rises to the maximum junction temperature of 150°C (up to which the CIPOS™ operates safely).

7.5 Heat sink selection guide

7.5.1 Required heat sink performance

If the power losses $P_{sw,i}$, $R_{th,J-C}$ and the maximum ambient temperature are known, the required thermal resistance of the heat sink and the thermal interface material can be calculated according to Figure 25 from

$$T_{J,max} = T_{A,max} + \sum_i P_{sw,i} \cdot R_{th,HS-A} + \sum_i P_{sw,i} \cdot R_{th,C-HS} + Max(P_{sw,i} \cdot R_{th,JC,i}) \quad (16)$$

For three phase bridges one can simply assume that all power switches dissipate the same power and they all have the same $R_{th,J-C}$. This leads to the required thermal resistance from case to ambient

$$R_{th,C-A} = R_{th,C-HS} + R_{th,HS-A} = \frac{T_{J,max} - P_{sw} \cdot R_{th,JC} - T_{A,max}}{\sum P_{sw}} \quad (17)$$

For example, the power switches of a washing machine drive dissipate 3.5W maximum each, the maximum ambient temperature is 50°C, the maximum junction temperature is 150°C and $R_{th,jC}$ is 3K/W. This results in

$$R_{th,C-A} \le \frac{150°C - 3.5W \cdot 3\frac{K}{W} - 50°C}{6 \cdot 3.5W} = 4.3\frac{K}{W}$$

If the heat sink temperature shall be limited to 100°C, an even lower thermal resistance is required:

$$R_{th,C-A} \le \frac{100°C - 50°C}{6 \cdot 3.5W} = 2.4\frac{K}{W}$$

Smaller heat sinks with higher thermal resistances may be acceptable if the maximum power is only required for a short time (times below the time constant of the thermal resistance and the thermal capacitance). However, this requires a detailed analysis of the transient power and temperature profiles. The larger the heat sink the larger it's thermal capacitance the longer does it take to heat up the heat sink.

7.5.2 Heat sink characteristics

Heat sinks are characterized by three parameters:

- Heat transfer from the power source to heat sink
- Heat transfer within the heat sink (to all the surfaces of the heat sink)
- Heat transfer from heat sink surfaces to ambient

7.5.2.1 Heat transfer from heat source to heat sink

There are two factors which need to be considered in order to provide a good thermal contact between power source and heat sink:

- **Flatness of the contact area.** Due to the unevenness of surfaces, a thermal interface material needs to be supplied between heat source and heat sink. However, such materials have a rather low thermal conductivity (<10K/W). Hence these materials should be as thin as possible. On the other hand, they need to fill out the space between heat source and heat sink. Therefore, the unevenness of the heat sink should be as low as possible. In addition, the particle size of the interface material must fit to the roughness of the module and the heat sink surfaces. Too large particle will unnecessarily increase the thickness of the interface layer and hence will increase the thermal resistance. Too small particles will not provide a good contact between the two surfaces and will lead to a higher thermal resistance as well.
- **Mounting pressure.** The higher the mounting pressure the better the interface material disperses and excessive interface material squeezes out resulting in a thinner interface layer with a lower thermal resistance.

7.5.2.2 Heat transfer within the heat sink

The heat transfer within the heat sink is mainly determined by:

- **Heat sink material.** The material needs to be a good thermal conductor. Most heat sinks are made of aluminum ($\lambda \approx 200W/(m*K)$). Copper is heavier and more expensive but also nearly twice as efficient ($\lambda \approx 400W/(m*K)$).
- **Fin thickness.** If the fins are too thin, the thermal resistance from heat source to fin is too high and the efficiency of the fin decreases. Hence it does not make sense to make the fins as thin as possible in order to spent more fins and therefore to increase the surface area.

7.5.2.3 Heat transfer from heat sink surface to ambient

The heat transfers to the ambient mainly by convection. The corresponding thermal resistance is defined as

$$R_{th,conv} = \frac{1}{\alpha \cdot A} \quad (18)$$

Where α is the heat transfer coefficient and A is the surface area.

Hence there are two important parameters:

• **Surface area.** Heat sinks require a huge surface area in order to easily transfer the heat to the ambient. However, as the heat source is assumed to be concentrated at a point and not uniformly distributed, the total thermal resistance of a heat sink does not change linearly with length. Also, increasing the surface area by increasing the number of fins does not necessarily reduce the thermal resistance as discussed in section 7.5.2.2.

• **Heat transfer coefficient (aerodynamics).** This coefficient is strongly depending on the air flow velocity as shown in Figure 28. If there is no externally induced flow one speaks of natural convection, otherwise from forced convection. Heat sinks with very small fin spacing do not allow a good air flow. If a fan is used, the fin gap may be lower than for natural convection as the fan forces the air through the space between the fins.

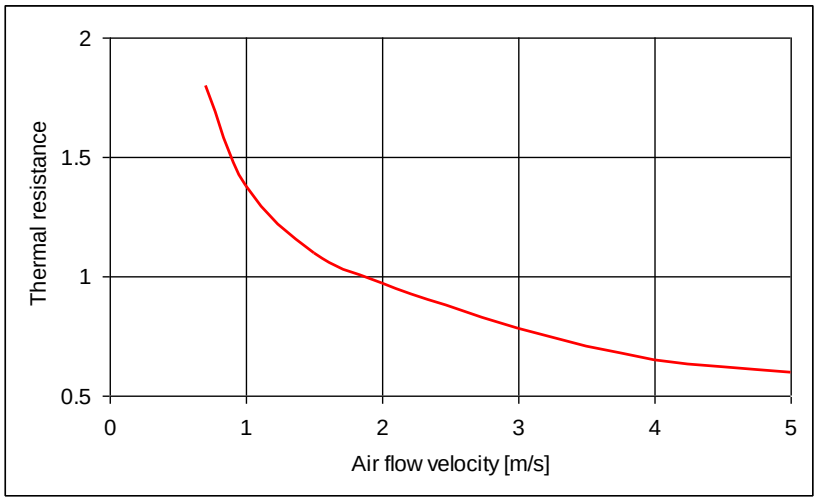


Figure 28. Thermal resistance as a function of the air flow velocity

Furthermore, in case of natural convection the heat sink efficiency depends on the temperature difference of heat sink and ambient (i.e. on the dissipated power). Some manufacturers, like Aavid thermalloy, provide a correction table which allows calculating the thermal resistance depending on the temperature difference. Figure 29 shows the heat sink efficiency degradation for natural convection as provided in [6]. Please note that the thermal resistance is 25% higher at 30W than at 75W.

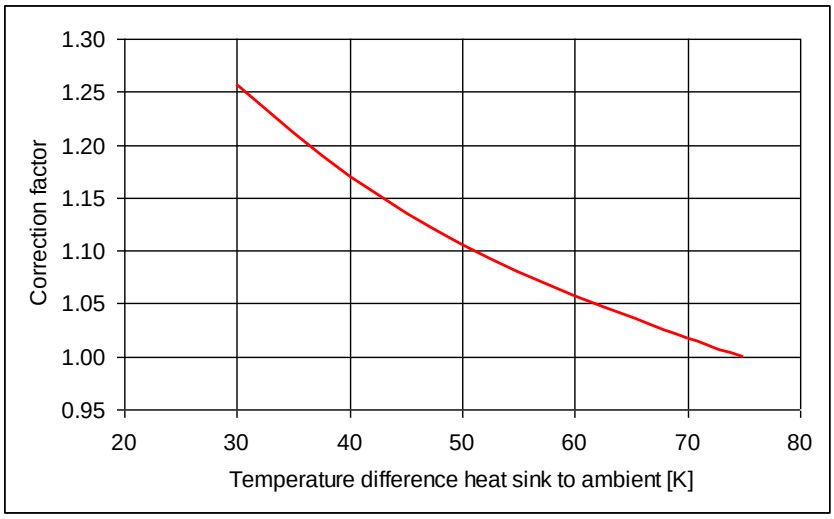


Figure 29. Correction factors for temperature

The positioning of the heat sink plays also an important role for the aerodynamics. In case of natural convection the best mounting attitude is with vertical fins as the heated air tends to move upwards due to buoyancy. Furthermore, one should make sure that there are no significant obstructions impeding the air flow.

Radiation occurs as well supporting the heat transfer from heat sink to ambient. In order to the increase radiated heat one can use anodized heat sinks with a black surface. However, this decreases the thermal resistance of the heat sink only by a few percent in case of natural convection. Radiated heat is negligible in case of forced convection. Hence blank heat sinks can be used if there is a fan used with the heat sink.

The discussions in this section clearly show that there cannot be a single thermal resistance value assigned to a certain heat sink.

7.5.3 Selecting a heat sink

Unfortunately there are no straightforward recipes for selecting heat sinks. Finding a sufficient heat sink will include an iterative process of choosing and testing heat sinks. In order to get a first rough estimation of the required volume of the heat sink, one can start with estimated volumetric thermal resistances as given in Table 19 (taken from [7]). This table gives only a first clue as the actual resistance may vary depending on many parameters like actual dimensions, type, orientation, etc.

Table 19. Volumetric thermal resistance

Flow conditions [m/s]	Volumetric Resistance [cm³ °C/W]
Natural Convection	500-800
1.0	150-250
2.5	80-150
5.0	50-80

One can roughly assume that the volume of a heat sink needs to be quadrupled in order to half it's thermal resistance. This gives a hint whether natural convection is sufficient for the available space or forced convection is required.

In order to get an optimized heat sink for a given application, one needs to contact heat sink manufacturers or consultants. Further hints and references can be found in [8].

When contacting heat sink manufacturers in order to find a suited heat sink, please take care under which conditions the given thermal resistance values are valid. They might be given either for a point source or for a heat source which is evenly distributed over the entire base area of the heat sink. Also take care that the fin spacing is optimized for the corresponding flow conditions.

8 Heat Sink Mounting and Handling Precaution

8.1 Heat sink mounting

8.1.1 General guidelines

An adequate heat sinking capability of the CIPOS™ is only achievable, if it is suitably mounted. This is the fundamental requirement in order to keep the electrical and thermal performance of the module. The following general points should be observed when mounting CIPOS™ on a heat sink. Verify the following points related to the heat sink:

a) There must be no burrs on aluminum or copper heat sinks.

b) Screw holes must be countersunk.

c) There must be no unevenness or scratches in the heat sink

d) The surface of the module must be completely in contact with the module.

e) There must be no oxidation nor stain or burrs on the heat sink surface

To improve the thermal conductivity, apply silicone grease to the contact surface between the CIPOS™ and heat sink. Spread a homogenous layer of silicone grease with a thickness of 100μm over the CIPOS™ substrate surface. Non-planar surfaces of the heat sink may require a thicker layer of thermal grease. Please refer here to the specifications of the heat sink manufacturer. It is important to note here, that the heat sink covers the complete backside of the module. There may be different functional behavior, if there is a portion of the backside of the module, which is not in contact with the heat sink.

To prevent a loss of heat dissipation effect due to warping of the substrate, tighten down the mounting screws gradually and sequentially while maintaining a left/right balance in pressure applied.

It must be assured by design of the application PCB, that the plane of the back side of the module and the plane of the heat sink are parallel in order to achieve minimal tensions of the package and an optimal contact of the module with the heat sink. Please refer to the mechanical specifications of the module given in the datasheets.

It is basics of good engineering to verify the function and thermal conditions by means of detailed measurements. It is best to use a final application inverter system, which is assembled with the final production process. This helps to ensure to achieve high quality applications.

8.1.1.1 Recommended tightening torque

As shown in Table 20, the tightening torque of M3 screws is specified for typically MS = 0.69N·m and maximum MS = 0.78N·m. The screw holes must be centered to the screw openings of the mold compound, so that the screws do not contact the mold compound. If an insulating sheet is used, use a sheet larger than the CIPOS™, and it should be aligned accurately when attached. It is important to ensure, that no air is enclosed by the insulating sheet. Generally speaking, insulating sheets are used in the following cases:

• When the ability to withstand primary and secondary voltages is required to achieve required safety standard.

• When CIPOS™ module must be insulated from the heat sink.

• When measures to reduce noise or other problems are required.

Table 20. Mechanical characteristics and ratings

Item	Condition	Limits			Unit
		Min.	Typ.	Max.	
Mounting Torque	Mounting Screw : M3	0.59	0.69	0.78	N·m
Device Flatness	(Note Figure 30)	-50	-	+100	μm
Heat Sink Flatness	(Note Figure 31)	-50	-	+100	μm
Weight		-	6.15	-	g

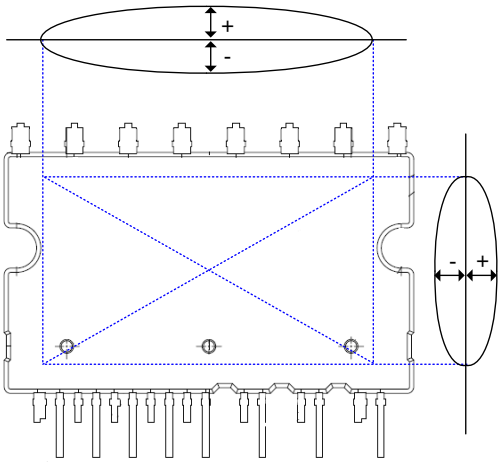


Figure 30. Device flatness measurement position

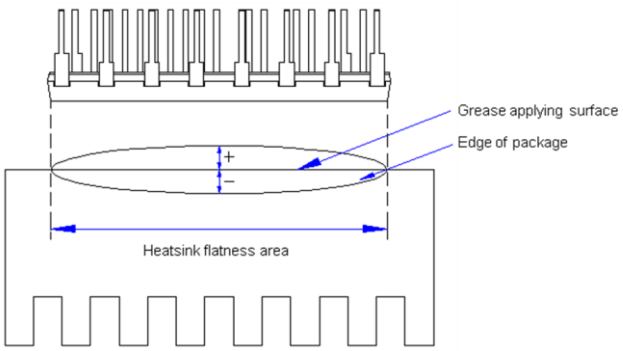


Figure 31. Heatsink flatness measurement position

8.1.1.2 Screw tightening to heat sink

The tightening of the screws is the main process of attaching the module to the heat sink. It is assumed, that an interface pad is attached to the heat sink face, which extends to the edge of the module and is located for the fixing holes. It is recommended, that M3 fixing screws are used in conjunction with a spring washer and a flat, rectangular washer. The spring washer must be assembled between the rectangular washer and the screw head. The screw torque must be monitored by the fixing tool.

Tightening Process:

- Align module with the fixing holes.
- Insert screw A with washers to touch only position (pre screwing).
- Insert screw B with washers (pre screwing).
- Tighten screw A to final torque.
- Tighten screw B to final torque.

Note : The pre screwing torque is set to 20~30% of maximum torque rating.

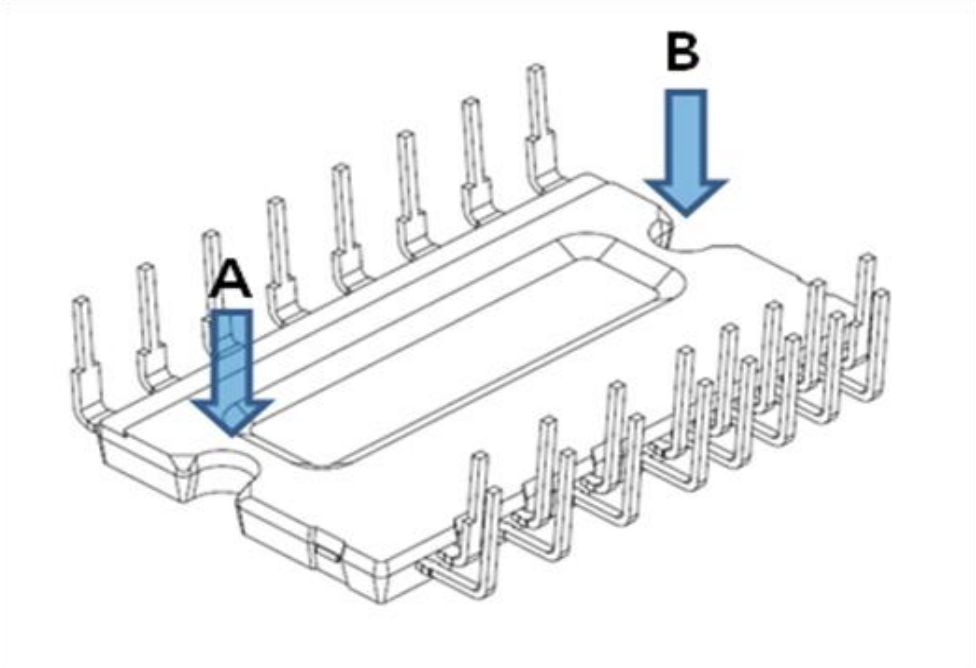


Figure 32. Recommended screw tightening order;
Pre screwing A→B, Final screwing A→B
8.1.4

8.1.2 Recommended heat sink shape

The shock or vibration through PCB or heat sink might cause the crack of package mounted on heat sink with screw. To avoid package broken or crack and to endure shock or vibration through PCB or heat sink, heat sink shape is recommended as shown in Figure 33. Heat sink need to be fixed on PCB with screw or eyelet.

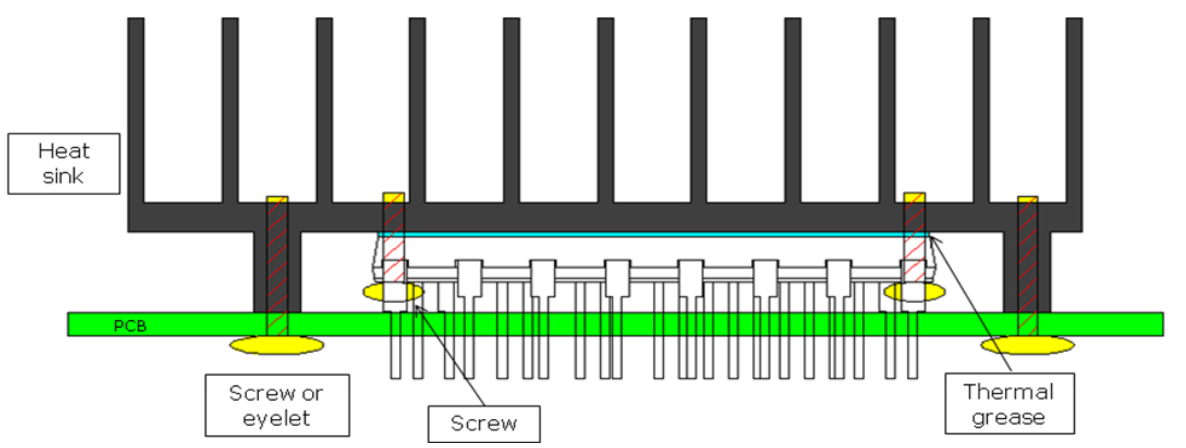


Figure 33. Recommended heat sink shape

8.2 Handling precaution

When installing a module to a heat sink, excessive uneven tightening force might apply stress to inside chips, which will lead to a broken or degradation of the device. An example of recommended fastening order is shown in Figure 32

- Do not over torque when mounting screws. Excessive mounting torque may cause the damage of the hole of module as well as the damage of screw and heat sink.
- Avoid one-side tightening stress, uneven mounting can cause the hole of module to be damaged.

To get effective heat dissipation, it is necessary to enlarge the contact area as much as possible, which minimizes the contact thermal resistance.

Properly, apply thermal conductive grease over the contact surface between the module and the heat sink, which is also useful for preventing the contact surface from corrosion. Furthermore the grease should be with stable quality and long term endurance within wide operating temperature range. Use a torque wrench to tighten to the specified torque rating. Exceeding the maximum torque limitation might cause a module to be damaged or degraded. Pay attention not to have any dirt remaining on the contact surface between the module and the heat sink. All equipment, which is used to handle or mount CIPOS™ modules must comply with the according standards in respect of ESD. This includes e.g. the transportation, storage and assembly. The module itself is an ESD sensitive device. It may therefore harm, in case of ESD shocks.

Don’t shake and handle with grabbing only heat sink, and especially don’t shock to PCB with grabbing only heat sink. That might cause the package crack or package broken.

8.3 Storage precaution

8.3.1 Recommended storage conditions

Temperature : 5 ~ 35℃

Relative humidity : 45 ~ 75%

- Avoid leaving that the CIPOS™ module is exposed to moisture or direct sunlight. especially, be careful during periods of rain or snow.
- Use storage areas where there is minimal temperature fluctuation.

Rapid temperature changes can cause moisture condensation on stored the CIPOS™ module, resulting in lead oxidation or corrosion as a result, lead solderability will be degraded

- Do not allow the CIPOS™ module to expose to corrosive gasses or in dusty conditions.
- Do not allow excessive external forces or loads to be applied to the CIPOS™ module while they are in storage

9 References

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