Control integrated Power System (CIPOS™)

Reference Board for CIPOS™ IKCS12G60DA

AN-CIPOS-Reference Board-3

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Power Management & Drives

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Reference Board for CIPOS™ IKCS12G60DA

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1 Introduction

This reference board is composed of the CIPOS™ IKCS12G60DA and its minimum peripheral components. It is designed for customers to evaluate the performance of CIPOS™ with simple connection of the control signals and power wires. **Figure 1** shows the external view of a reference board for IKCS12F60DA.

This application note describes how to design the key parameters and PCB layout.

Figure 1 Reference board for CIPOS™ IKCS12G60DA

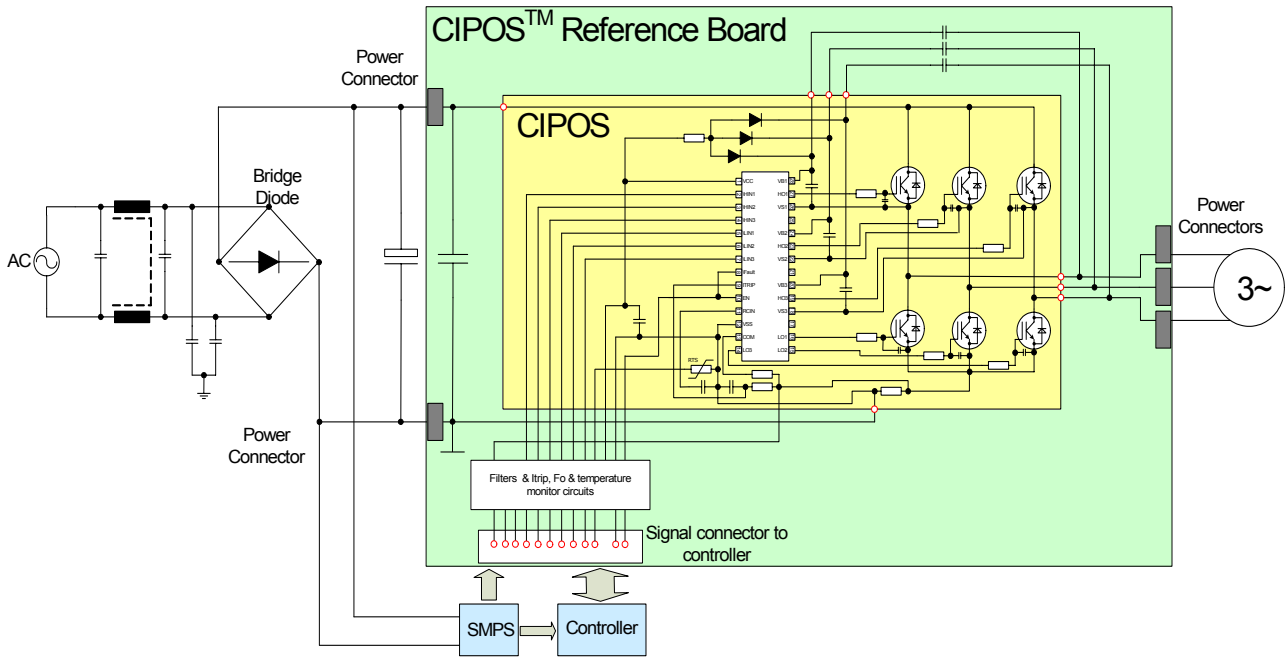

Figure 2 Application example

2 Schematic

Figure 3 shows a circuitry of reference board for CIPOS™ IKCS12G60DA.

Reference board consists of interface circuit, bootstrap capacitors, snubber capacitor, short-circuit protection, over-temperature protection and fault output circuit. The CIPOS™ includes bypass capacitors of 100nF at each Vcc and VBS, so the external bypass capacitors are not necessary. And the internal bypass capacitors are located very close to the drive IC, thus this is good advantage to prevent malfunction by noise.

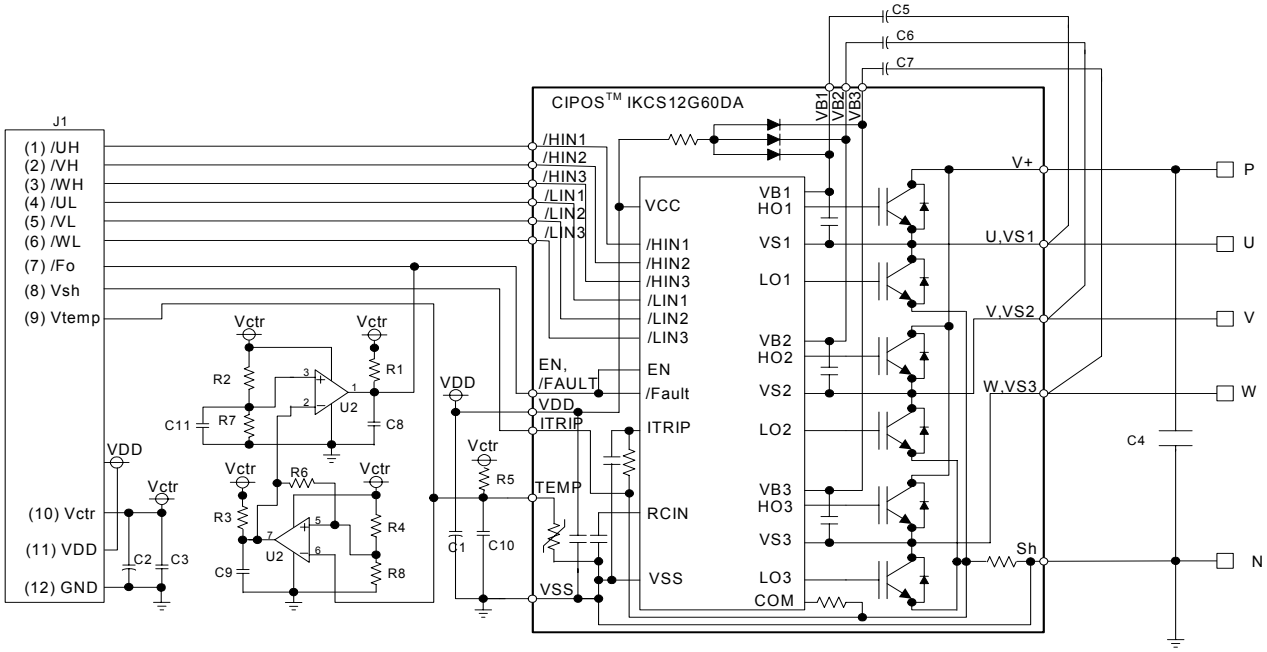

Figure 3 Circuit of reference board

Note :

Vctr denotes the controller supply voltage such as 5V or 3.3V for MCU or DSP.

3 External Connection

3.1 Signal Connector (J1)

Pin	Name	Description
1	/UH	High side control signal input of U phase
2	/VH	High side control signal input of V phase
3	/WH	High side control signal input of W phase
4	/UL	Low side control signal input of U phase
5	/VL	Low side control signal input of V phase
6	/WL	Low side control signal input of W phase
7	/Fo	Fault output signal
8	Vsh	Shunt voltage sensing signal
9	Vtemp	Temperature sensing signal of CIPOS™
10	Vctr	External control voltage (5V or 3.3V)
11	VDD	External 15V supply voltage
12	GND	Ground

3.2 Power Connector

Pin	Description
U	Output terminal of U-phase
V	Output terminal of V-phase
W	Output terminal of W-phase
P	Positive terminal of DC-link voltage
N	Negative terminal of DC-link voltage

4 Key Parameters Design Guide

4.1 Circuit of Input Signals ($\overline{\text{LIN}}$, $\overline{\text{HIN}}$)

The input signals can be either TTL- or CMOS-compatible. The logic levels can go down to 3.3V. The maximum input voltage of the pins is internally clamped to 10.5 V. However, the recommended voltage range of input voltage is up to 5V. The control pins LIN and HIN are active low.

They all have an internal pull-up structure with a pull-up resistor value of nominal 75 kΩ. The integrated pull-up resistors are designed to pull up the internal structures, so that the IC can control CIPOS™ safely.

The input noise filter inside CIPOS™ suppresses short pulse and prevents the driven IGBT from excessive switching loss. The input noise filter time is typically 270ns. This means that an input signal must stay on its level for this period of time in order that the state change is processed correctly.

And as shown in **Figure 4**, CIPOS™ can be connected directly to controller thanks to internal pull up resistor and input noise filter.

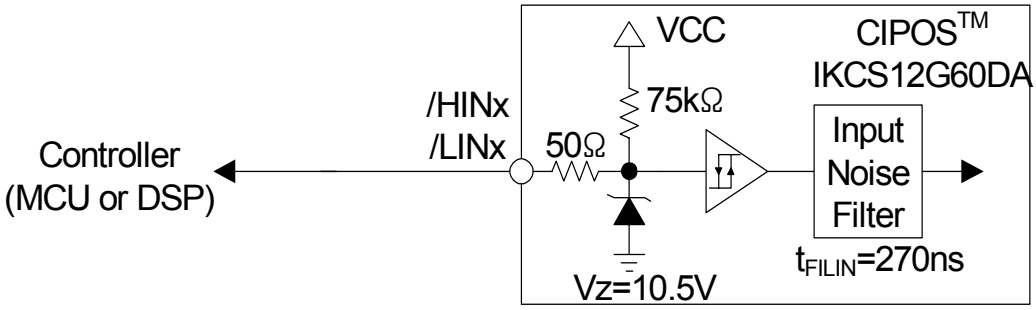

Figure 4 Internal input structure of CIPOS™

4.2 Bootstrap Capacitor

Bootstrapping is a common method of pumping charges from a low potential to a higher one. With this technique a supply voltage for the floating high side sections of the gate drive can be easily established according to **Figure 5**. It is only the effective circuit shown for one of the three half bridges. The bootstrap resistor R_{BS} is connected to each of the three bootstrap diodes in the module to limit current. Please refer to the datasheet and application note for the internal circuit and bootstrapping method in detail.

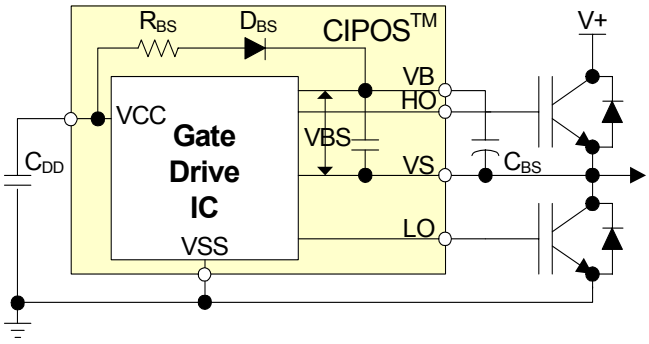

Figure 5 Bootstrap circuit for the supply of a high side gate drive

A low leakage current of the high side section is very important in order to keep the bootstrap capacitors small. The C_{BS} discharges mainly by the following machanisms:

- Quiescent current to the high side circuit in the IC
- Gate charge for turning high side IGBT on
- Level-shift charge required by level shifters in the IC
- Leakage current in the bootstrap diode
- C_{BS} capacitor leakage current (ignored for non-electrolytic capacitor)
- Bootstrap diode reverse recovery charge

The calculation of the bootstrap capacitor results in

$$C_{BS} = \frac{I_{leak} \times t_p}{\Delta v_{BS}}$$

with I_{leak} being the maximum discharge current of C_{BS}, t_P the maximum on pulse width of high side IGBT and Δv_{BS} the voltage drop at the bootstrap capacitor within a switching period.

Practically, the recommended leakage current is 1mA of I_{leak} for CIPOS™.

Figure 6 shows the curve corresponding to above equation for a continuous sinusoidal modulation, if the voltage ripple Δv_{BS} is 0.1V. The recommended bootstrap capacitance for a continuous sinusoidal modulation method is therefore in the range up to 4.7µF for most switching frequencies. In other pwm method case like a discontinuous sinusoidal modulation, tp must be set the longest period of the low side IGBT off.

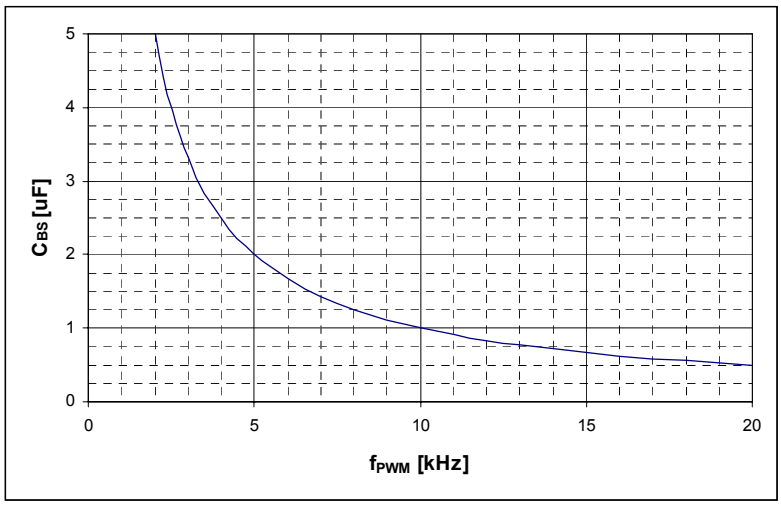

Figure 6 Size of the bootstrap capacitor as a function of the switching frequency f_{PWM}

4.3 Short-Circuit Protection

As shown in **Figure 7**, short-circuit protection comes to be achieved by CIPOS™ internal circuit. Typical current trip level is about 22.5A. When sensing voltage through shunt resistor exceeds 0.45V, fault output is to be activated and internal 6 IGBTs are turned fully off within less than 5us of short circuit withstand time(t_{SC}) in datasheet. The internal RC filter (0.47kΩ and 2.2nF) should be necessary in SC sensing circuit to prevent malfunction of SC protection due to noise interference. **Figure 8** shows timming chart of short circuit protection.

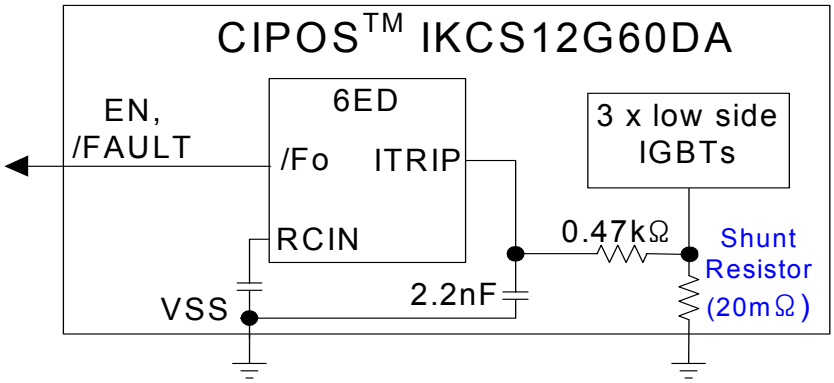

Figure 7 Short-circuit protection circuit

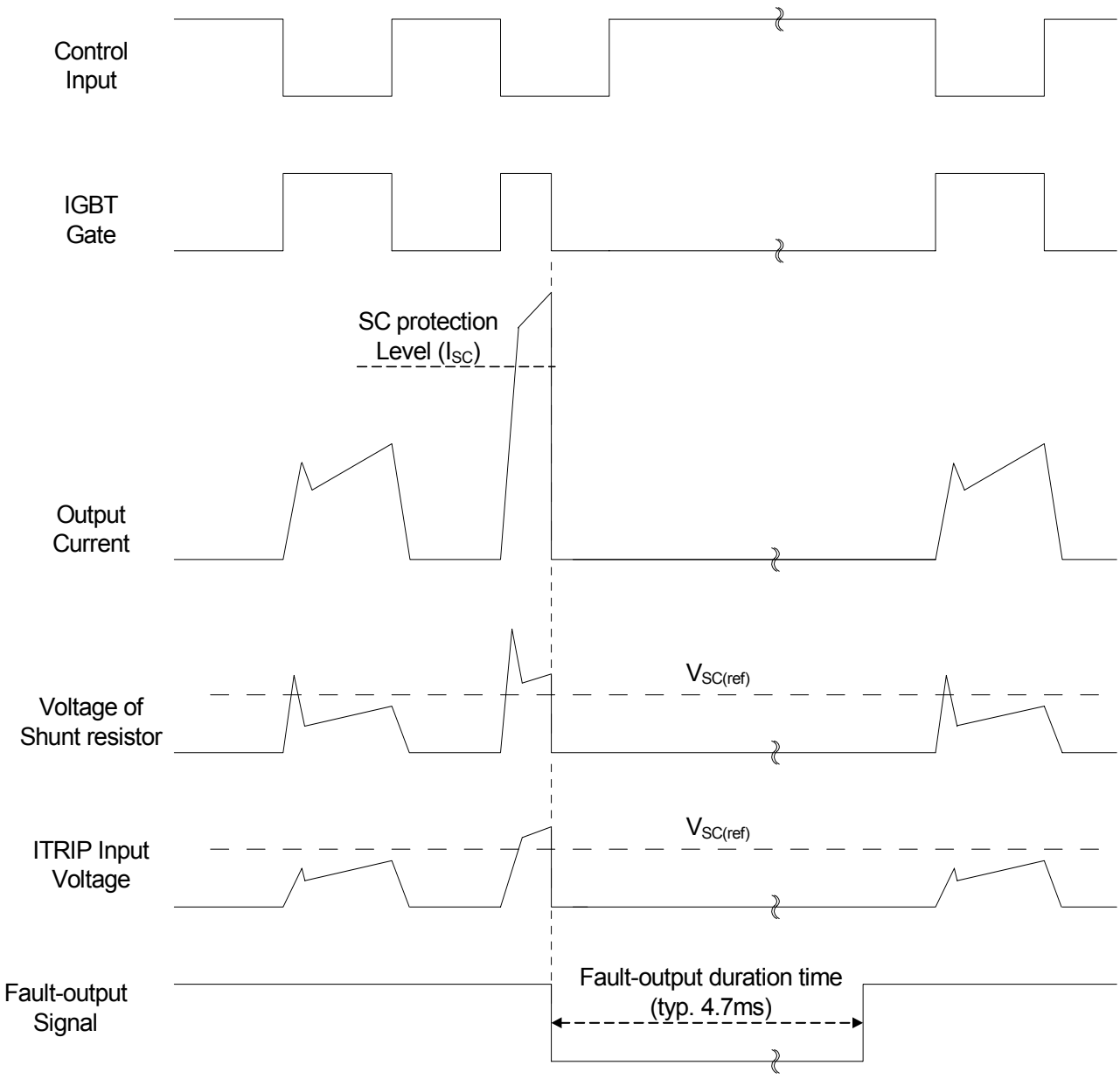

Figure 8 Timing chart of SC protection

4.4 Over-Temperature Protection

The CIPOS™ includes NTC of 100kΩ at 25°C. The NTC should be pulled up to 5V or 3.3V with external resistor (R5), and V_{TEMP} is determined by voltage divider (R4, R8). R6 is used for making hysteresis input to the comparator.

For example, when the control voltage Vctr is 5V or 3.3V, R5=20kΩ , R4=7.5kΩ , R8=2kΩ and R6=100kΩ , then V_{TEMP} at 100°C of NTC temperature is 1.04$V_{typ.}$at Vctr=5V and 0.68V at Vctr=3.3V, and the set level of over-temperature protection at NTC is about 100°C as shown in **Figure 9** and **Figure 10**.

After over temperature protection is set, operating mechanism of this function is same as short-circuit protection like fault out and internal 6 IGBTs shut down. Therefore, please refer to the chapter 4.3.

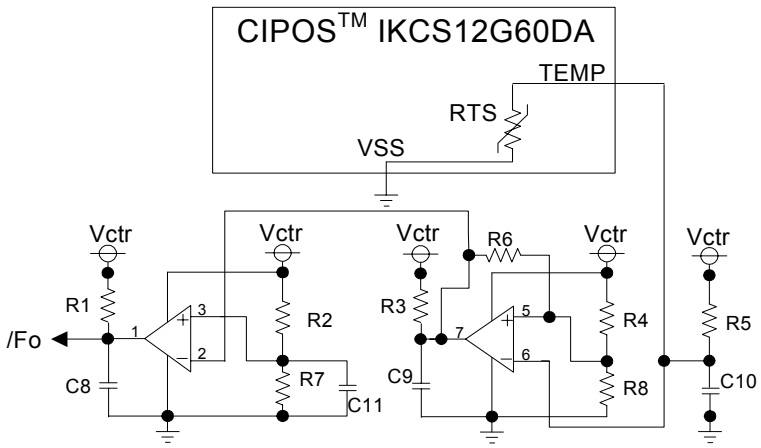

Figure 9 Over-temperature protection with NTC

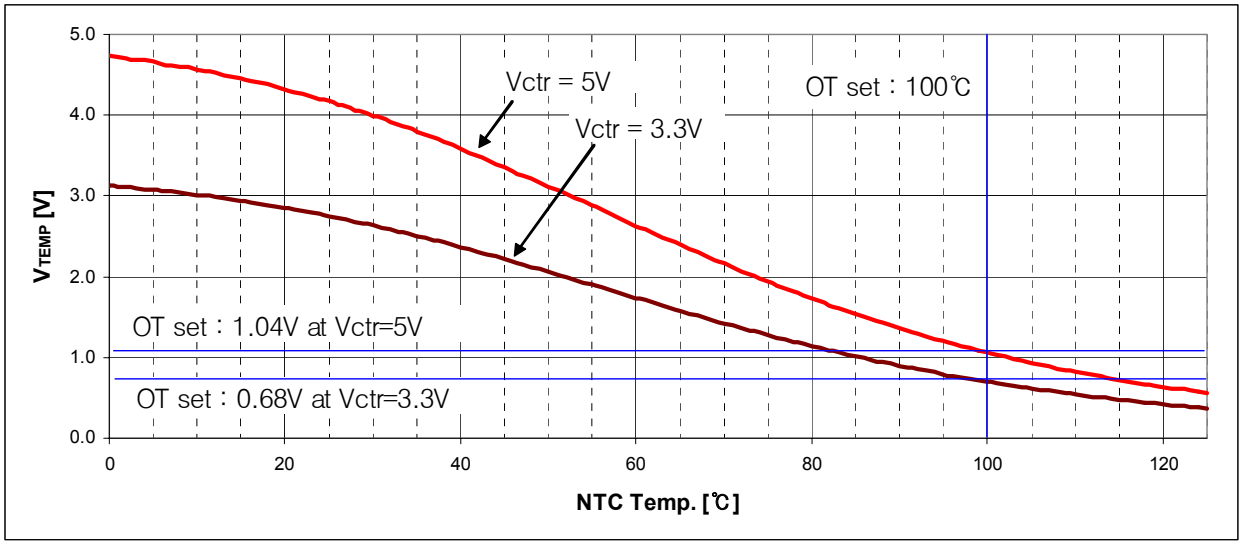

Figure 10 Voltage of TEMP pin according to NTC temperature

5 Part List

Symbol	Components	Note
R1	2kΩ, 1/8W, 5%	Pull-up resistors for comparator output ($\overline{Fo}$)
R2	10kΩ, 1/8W, 5%	Voltage devider for reference voltage
R3	10kΩ, 1/8W, 5%	Pull-up resistor for comparator output
R4	7.5kΩ, 1/8W, 1%	Voltage devider for V_{TEMP}
R5	20kΩ, 1/8W, 1%	Pull-up resistor for temperature sensing
R6	100kΩ, 1/8W, 1%	Resistor for signal stable of comparator output
R7	10kΩ, 1/8W, 5%	Voltage devider for reference voltage
R8	2kΩ, 1/8W, 1%	Voltage devider for V_{TEMP}
C1	220uF 35V	+15V Bias voltage source capacitor
C2	100uF 16V	+5V Bias voltage source capacitor
C3	100nF 25V	Bypass capacitor for +5V
C4	0.1uF 630V	Snubber capacitor
C5 ~ C7	4.7uF 35V	Bootstrap capacitors
C8	1nF 25V	Bypass capacitor for fault-output signal
C9	100pF 25V	Bypass capacitor for comparator output
C10	100nF 25V	Bypass capacitor for NTC temperature sensing
C11	100pF 25V	Bypass capacitor for reference voltage
U1	CIPOS™	Control Intergrated Power System
U2	LM393	Dual comparator for fault-output signal
J1	12pin Connector	Signal & power supply connector
U,V,W,P,N	Fasten Tap	Power terminals

6 PCB Design Guide

In general, there are several issues to be considered when designing an inverter board as below lists.

- Separate signal line and power line
- Low stray inductive connection
- Isolation distance
- Component placement

This chapter explains above considerations and method for the layout design.

6.1 Main Consideration of Layout Design

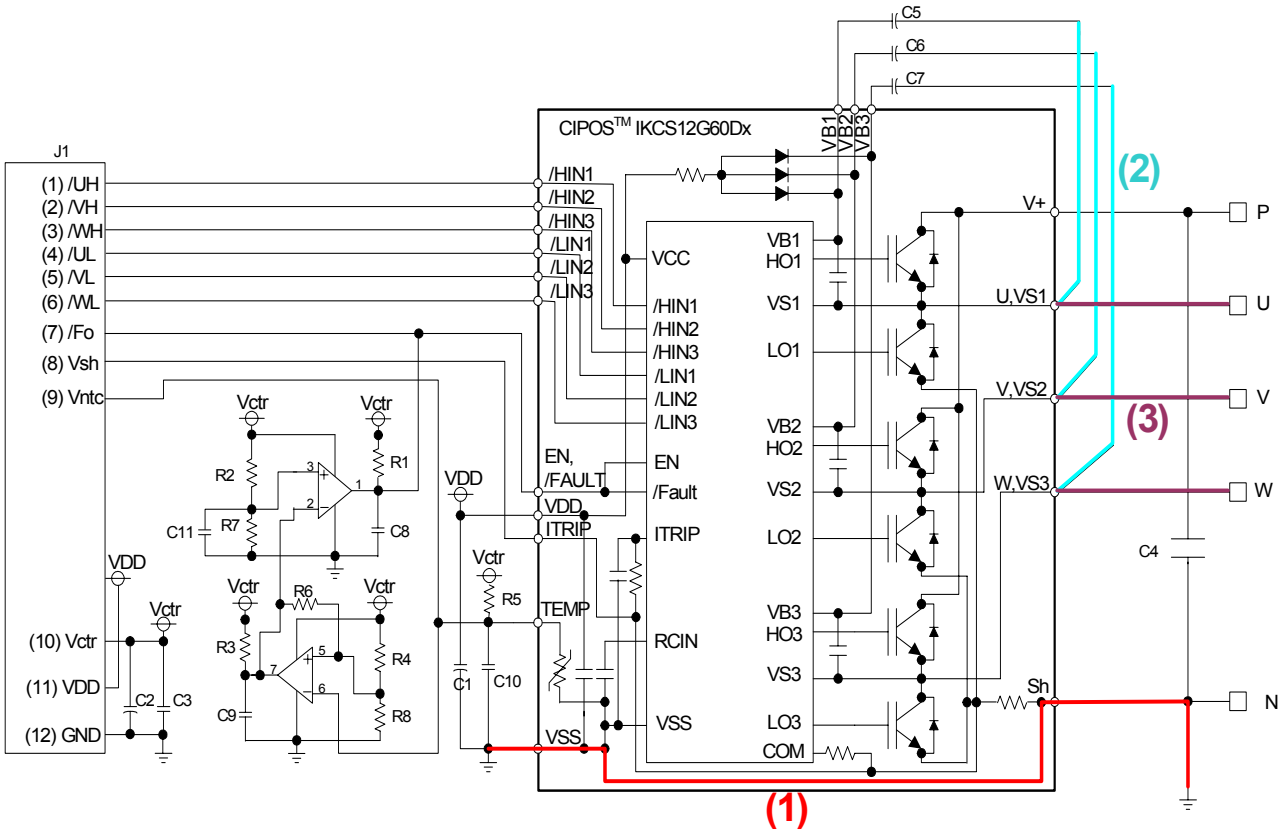

Figure 11 Example of interface circuit

Note.

1. As shown in (1), signal GND and Power GND are connected internally in CIPOS™, therefore, it's not necessary to be connected on the reference board.

3. All of the bypass capacitors should be placed as close to the CIPOS™ as possible.

4. VS(2) and main output(3) patterns should be separated.

5. The snubber capacitor (C4) should be placed as close to the CIPOS™ as possible.

6.2 PCB Design Guide

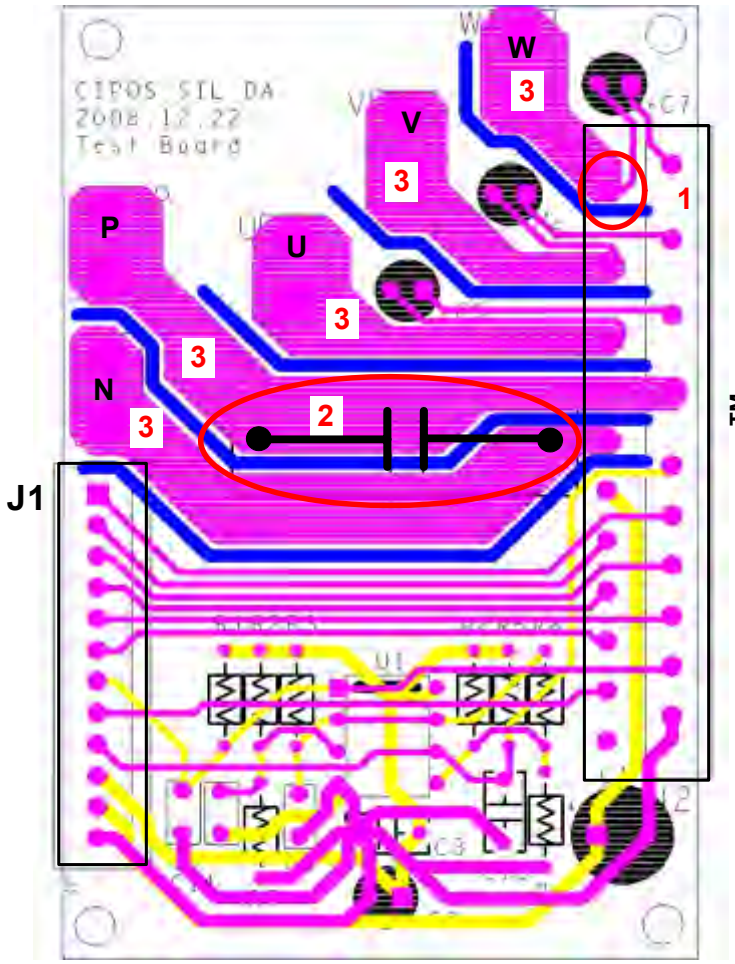

Figure 12 Example of PCB layout

Note.

1. Negative pin of bootstrap capacitor should be connected to output pin(U,V,W) directly and seperated from the main patterns of output.
2. The snubber capacitor should be placed as close to the terminals as possible.
3. The power patterns of U,V,W,P and N should be designed on both layer with vias to cover the high current and there should be kept the isolation distance among the power patterns over 2.5mm.

6.3 Layout of Reference Board

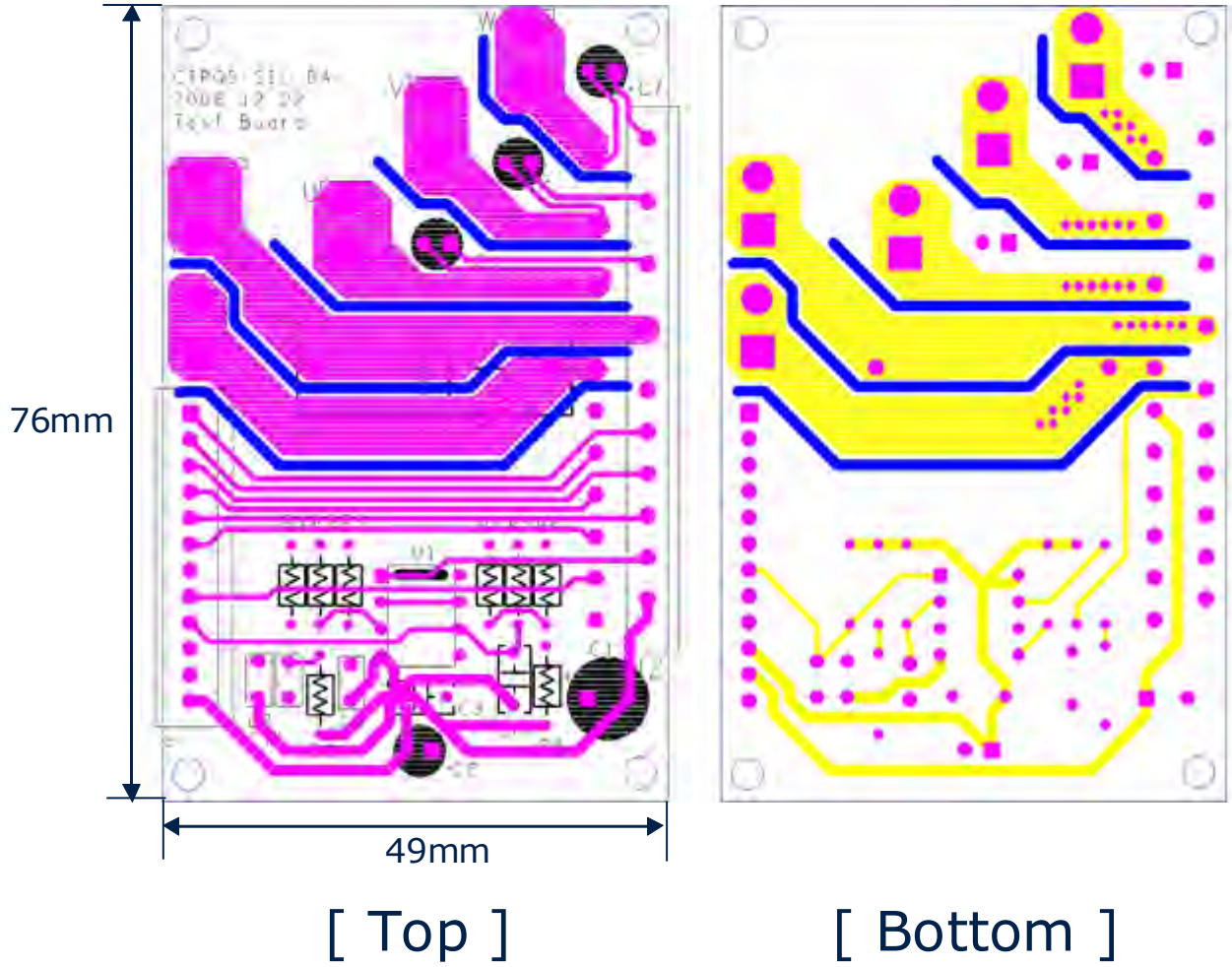

Figure 13 Layout of reference board

Note.

1. All components are placed on the top layer.
2. There are milling profiles in blue line to keep the isolation distance between power patterns, where the isolation distance is not enough.

7 Reference

[1] **Infineon Technologies:** CIPOS™ IKCS12G60DA; Preliminary Datasheet Rev. 2; Infineon Technologies, Germany, 2008.

[2] **Infineon Technologies:** Reference Board for CIPOS™ IKCSxxF60B(2)x; Application Note V 1.0; Infineon Technologies, Korea, 2008