Application Note, V1.0, Feb. 2009

Control integrated Power System (CIPOS™)

Reference Board for CIPOS™ IKCSxxF60F2x

AN-CIPOS-Reference Board-4

Authors: Junbae Lee

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Power Management & Drives

Never stop thinking

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Reference Board for CIPOS™ IKCSxxF60F2x

Revision History: 2009-02 V1.0

Previous Version:

Page	Subjects (major changes since last version)

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Edition 2009-02

Published by
Infineon Technologies Korea
Seoul, South Korea

1 Introduction

This reference board is composed of the CIPOS™ IKCSxxF60F2x, its minimum peripheral components and single shunt resistor. It is designed for customers to evaluate the performance of CIPOS™ with simple connection of the control signals and power wires.

The electrical circuit of both reference boards for IKCSxxF60F2A and IKCSxxF60F2C is exactly same, however, PCB layout of them is different due to the difference of lead forming type between IKCSxxF60F2A and IKCSxxF60F2C. **Figure 1** and **Figure 2** show the external view of two kinds of reference boards.

This application note describes how to design the key parameters and PCB layout.

Figure 1 Reference board for CIPOS™ IKCSxxF60F2A

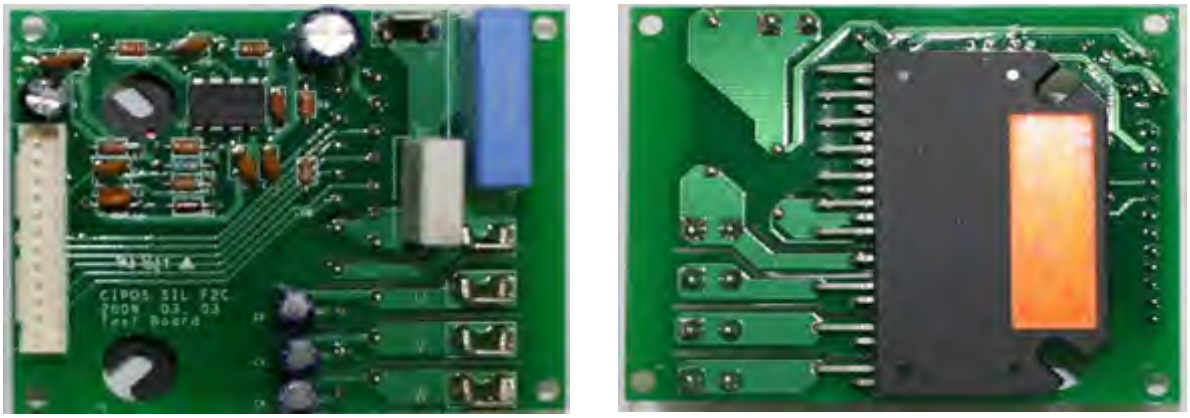

Figure 2 Reference board for CIPOS™ IKCSxxF60F2C

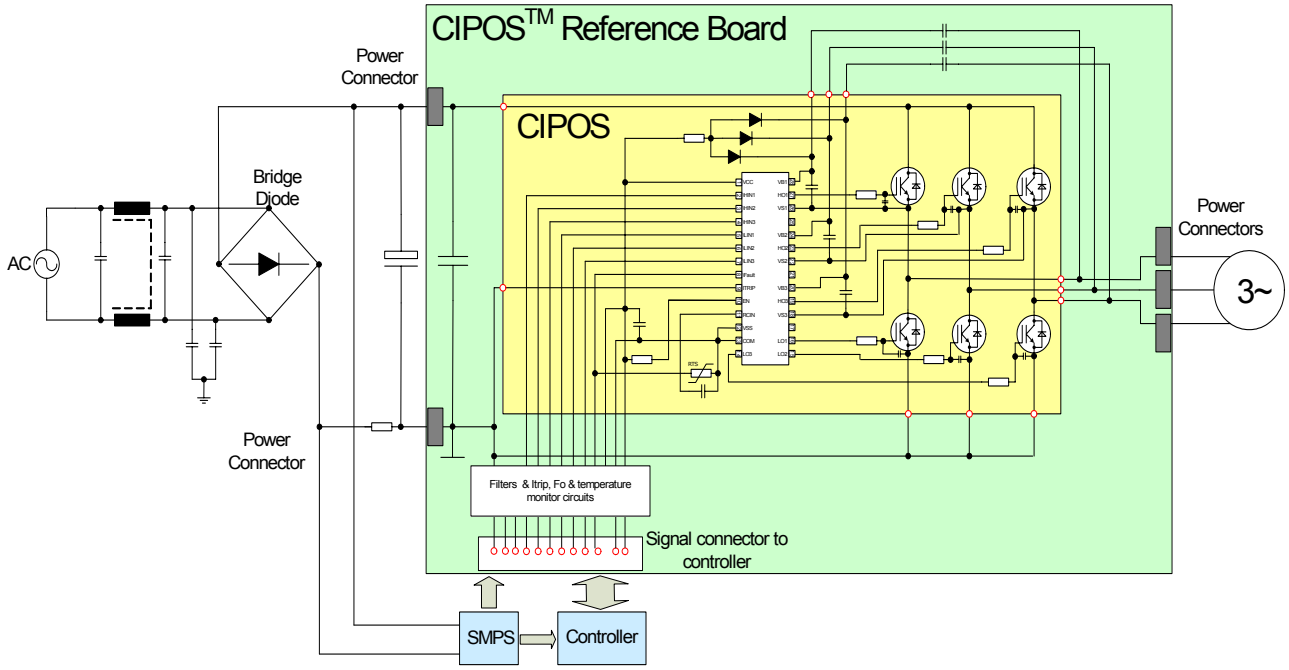

Figure 3 Application example

2 Schematic

Figure 4 shows a circuitry of the reference board for CIPOS™ IKCSxxF60F2x.

The reference board consists of interface circuit, bootstrap capacitors, snubber capacitor, short-circuit protection, over-temperature protection, fault output circuit and single shunt resistor. The CIPOS™ includes bypass capacitors of 100nF at each Vcc and VBS, so the external bypass capacitors are not necessary. And the internal bypass capacitors are located very close to the drive IC, thus this is good advantage to prevent malfunction by noise.

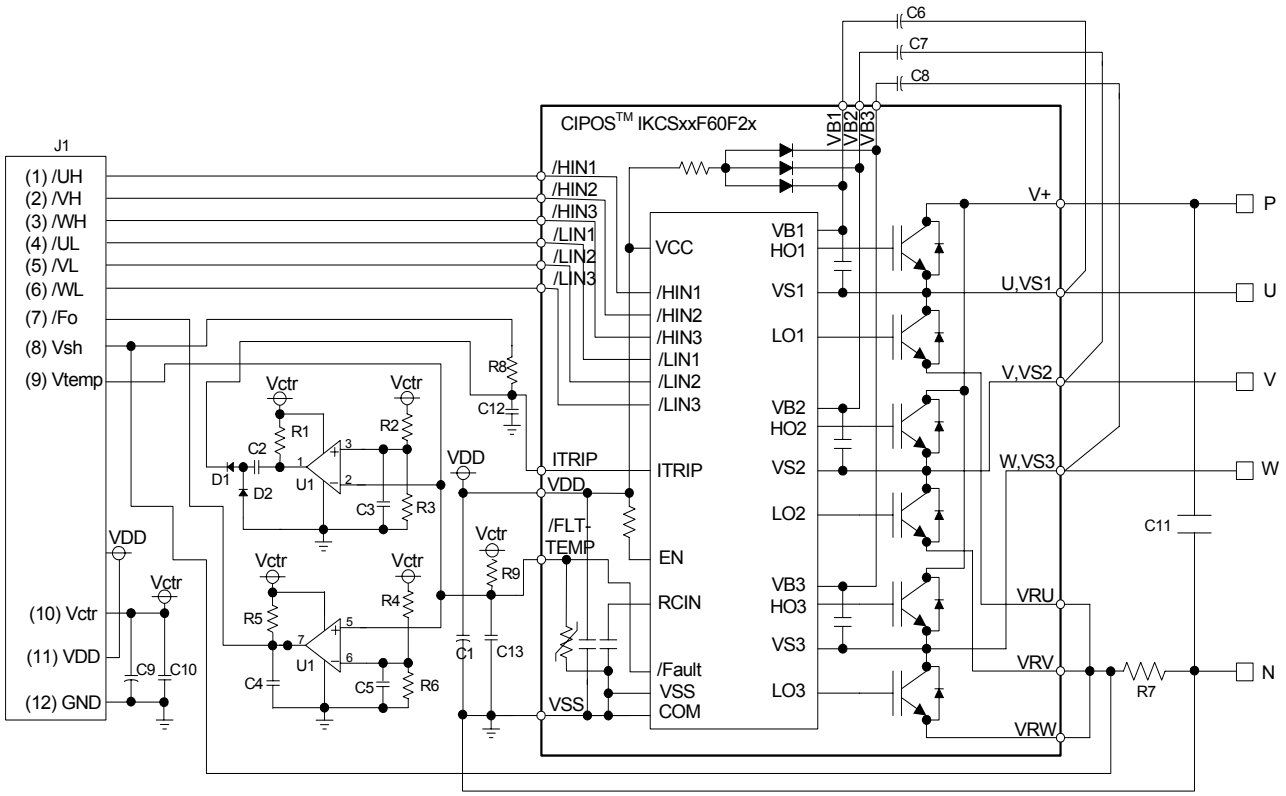

Figure 4 Circuit of the reference board

Note :

Vctr denotes the controller supply voltage such as 5V or 3.3V for MCU or DSP.

3 External Connection

3.1 Signal Connector (J1)

Pin	Name	Description
1	/UH	High side control signal input of U phase
2	/VH	High side control signal input of V phase
3	/WH	High side control signal input of W phase
4	/UL	Low side control signal input of U phase
5	/VL	Low side control signal input of V phase
6	/WL	Low side control signal input of W phase
7	/Fo	Fault output signal
8	Vsh	Shunt voltage sensing signal
9	Vtemp	Temperature sensing signal of CIPOS™
10	Vctr	External control voltage (5V or 3.3V)
11	VDD	External 15V supply voltage
12	GND	Ground

3.2 Power Connector

Pin	Description
U	Output terminal of U-phase
V	Output terminal of V-phase
W	Output terminal of W-phase
P	Positive terminal of DC-link voltage
N	Negative terminal of DC-link voltage

4 Key Parameters Design Guide

4.1 Circuit of Input Signals ($\overline{\text{LIN}}$, $\overline{\text{HIN}}$)

The input signals can be either TTL- or CMOS-compatible. The logic levels can go down to 3.3V. The maximum input voltage of the pins is internally clamped to 10.5 V. However, the recommended voltage range of input voltage is up to 5V. The control pins LIN and HIN are active low.

They all have an internal pull-up structure with a pull-up resistor value of nominal 75 kΩ. The integrated pull-up resistors are designed to pull up the internal structures, so that the IC can control CIPOS™ safely.

The input noise filter inside CIPOS™ suppresses short pulse and prevents the driven IGBT from excessive switching loss. The input noise filter time is typically 270ns. This means that an input signal must stay on its level for this period of time in order that the state change is processed correctly.

And as shown in **Figure 5**, CIPOS™ can be connected directly to controller thanks to internal pull up resistor and input noise filter.

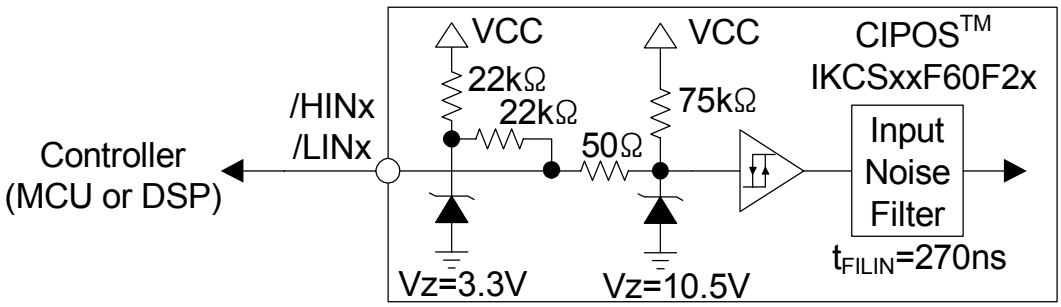

Figure 5 RC-filter of input signals and pull-up circuit

4.2 Bootstrap Capacitor

Bootstrapping is a common method of pumping charges from a low potential to a higher one. With this technique a supply voltage for the floating high side sections of the gate drive can be easily established according to **Figure 6**. It is only the effective circuit shown for one of the three half bridges. The bootstrap resistor R_{BS} is connected to each of the three bootstrap diodes in the module to limit current. Please refer to the datasheet and application note for the internal circuit and bootstrapping method in detail.

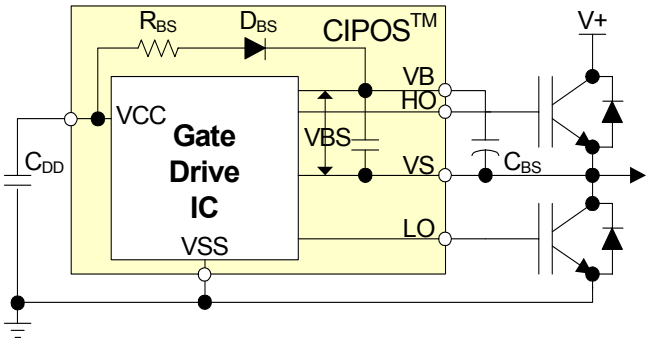

Figure 6 Bootstrap circuit for the supply of a high side gate drive

A low leakage current of the high side section is very important in order to keep the bootstrap capacitors small. The C_{BS} discharges mainly by the following mechanisms:

- Quiescent current to the high side circuit in the IC
- Gate charge for turning high side IGBT on
- Level-shift charge required by level shifters in the IC
- Leakage current in the bootstrap diode
- C_{BS} capacitor leakage current (ignored for non-electrolytic capacitor)
- Bootstrap diode reverse recovery charge

The calculation of the bootstrap capacitor results in

$$C_{BS} = \frac{I_{leak} \times t_p}{\Delta v_{BS}}$$

with I_{leak} being the maximum discharge current of C_{BS}, t_P the maximum on pulse width of high side IGBT and Δv_{BS} the voltage drop at the bootstrap capacitor within a switching period.

Practically, the recommended leakage current is 1mA of I_{leak} for CIPOS™.

Figure 7 shows the curve corresponding to above equation for a continuous sinusoidal modulation, if the voltage ripple Δv_{BS} is 0.1V. The recommended bootstrap capacitance for a continuous sinusoidal modulation method is therefore in the range up to 4.7µF for most switching frequencies. In other pwm method case like a discontinuous sinusoidal modulation, tp must be set the longest period of the low side IGBT off.

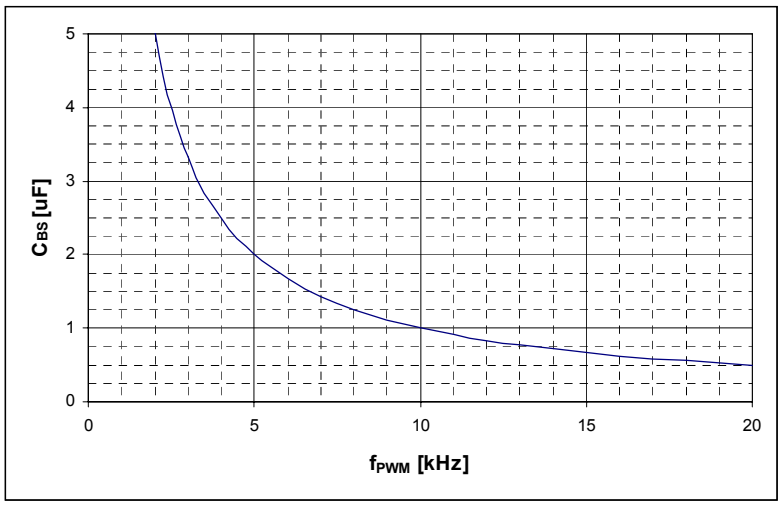

Figure 7 Size of the bootstrap capacitor as a function of the switching frequency f_{PWM}

4.3 Short-Circuit Protection

The reference board has a comparator circuit to prevent unintentional fault-output signal from voltage drop of /FLT_TEMP according to temperature increase. The SC protection level is decided by ITRIP positive going threshold voltage $V_{IT,TH+}$ in CIPOS™ and shunt resistance. When ITRIP voltage exceeds $V_{IT,TH+}$, CIPOS™ turns off 6 IGBTs and fault-output is activated during fault-output duration time, typ. 4.7ms.

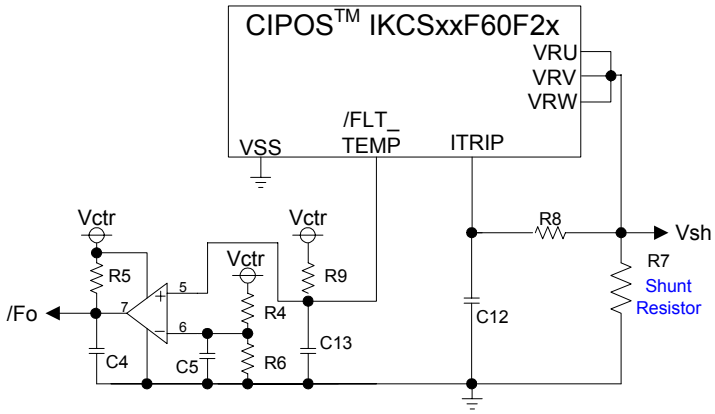

Figure 8 Short-circuit protection circuit

4.3.1 Shunt Resistor Selection

The value of shunt resistor is calculated by the following equation.

$$R_{SH} = \frac{V_{IT,TH+}}{I_{SC}}$$

Where $V_{IT,TH+}$ is the ITRIP positive going threshold voltage of CIPOS™ and I_{SC} is the current of SC detection level. $V_{IT,TH+}$ is $0.45V_{typ.}$.

The maximum value of SC protection level should be set less than the repetitive peak collector current in the datasheet considering the tolerance of shunt resistor.

For example, the maximum peak collector current of IKCS12F60F2A is $18A_{peak}$,

$$R_{SH(min)} = 0.45/18 = 0.025\Omega$$

So the recommended value of shunt resistor is over 25mΩ for IKCS12F60F2A.

For the power rating of the shunt resistor, the below lists should be considered.

- Maximum load current of inverter (I_{rms})
- Shunt resistor value at Tc=25°C (R_{SH})
- Power derating ratio of shunt resistor at T_{SH}=100°C
- Safety margin

And the power rating is calculated by following equation.

$$P_{SH} = \frac{I_{rms}^2 R_{SH} \times margin}{Derating\ ratio}$$

For example, In case of IKCS12F60F2A and R_{SH}=25mΩ

- Max. load current of inverter : $6A_{rms}$
- Power derating ratio of shunt resistor at T_{SH}=100°C : 80%
- Safety margin : 30%

$$P_{SH} = \frac{6^2 \times 0.025 \times 1.3}{0.8} = 1.46W$$

So the proper power rating of shunt resistor is over 2W.

Based on the previous equations, conditions, and calaulation method, minimum shunt resistance and resistor power according to all kinds of CIPOS™ IKCSxxF60F2x products are introduced as shown in below table.

It's noted that a proper resistance and its power over than minimum values should be chosen considering over-current protection level required in the application set.

Products	Maximum Peak Current	**Minimum** shunt resistance, $\mathbf{R_{SH}}$	**Minimum** shunt resistor power, $\mathbf{P_{SH}}$
IKCS22F60F2x	45	10mΩ	4W
IKCS17F60F2x	30	15mΩ	3W
IKCS12F60F2x	18	25mΩ	2W
IKCS08F60F2x	12	38mΩ	1W

4.3.2 Delay Time

The RC filter should be necessary in SC sensing circuit to prevent malfunction of SC protection from noise interference. The RC time constant is determined by applying time of noise and the withstand time capability of IGBT.

When the current on shunt resistor exceeds SC protection level(I_{sc}), this voltage is applied to the ITRIP pin of CIPOS™ via the RC filter. The filter delay time(t1) that the input voltage of ITRIP pin rises to the ITRIP positive threshold voltage is caused by RC filter time constant.

In addition there are the Input filter time of Itrip(t2) and shutdown propagation delay of Itrip(t3). Please refer to the below table.

Item	min.	typ.	max.	unit
Input filter time of Itrip (t2)	155	225	380	ns
Shutdown propagation delay (t3)	-	900	-	ns

Therefore, the total delay time from occurrence of SC to shutdown of the IGBT gate becomes

$$t_{Total} = 2xt1 + t2 + t3$$

The total delay should be less than 5us of short circuit withstand time(t_{SC}) in datasheet. Thus, RC time constant should be set in the range of 1~2us. It is recommended that R of 1.8kΩ and C of 1nF.

4.4 Over-Temperature Protection

IKCSxxF60F2x has one pin for both falut-output and TEMP sensing. So the reference board has a comparator to prevent unintentional fault-output signal from voltage drop of /FLT_TEMP according to temperature increase. The CIPOS™ includes NTC of 100kΩ at 25°C. The NTC should be pulled up to 5V or 3.3V with external resistor (R9), and V_{TEMP} is determined by voltage divider (R2, R3). For example, when the control voltage Vctr is 5V or 3.3V, R9=12kΩ , R2=5.6kΩ and R3=2.4kΩ , then V_{TEMP} at about 100°C of NTC temperature is $1.5V_{typ.}$at Vctr=5V and 1V at Vctr=3.3V, and the set level of over-temperature protection at NTC is about 100°C as shown in **Figure 9** and **Figure 10**.

After over temperature protection is set, fault out is once activated during typical 4.7ms and internal 6 IGBTs are shut down.

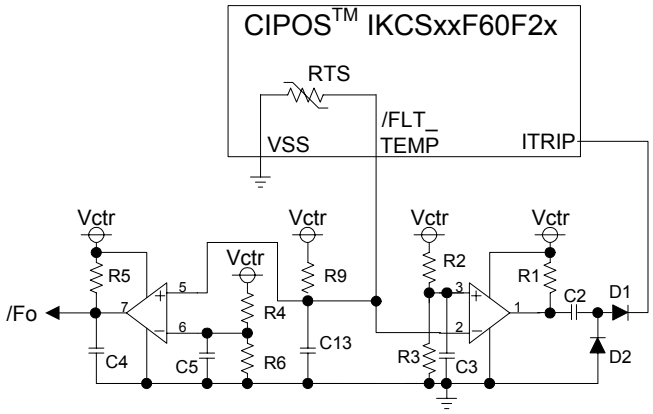

Figure 9 Over-temperature protection with NTC

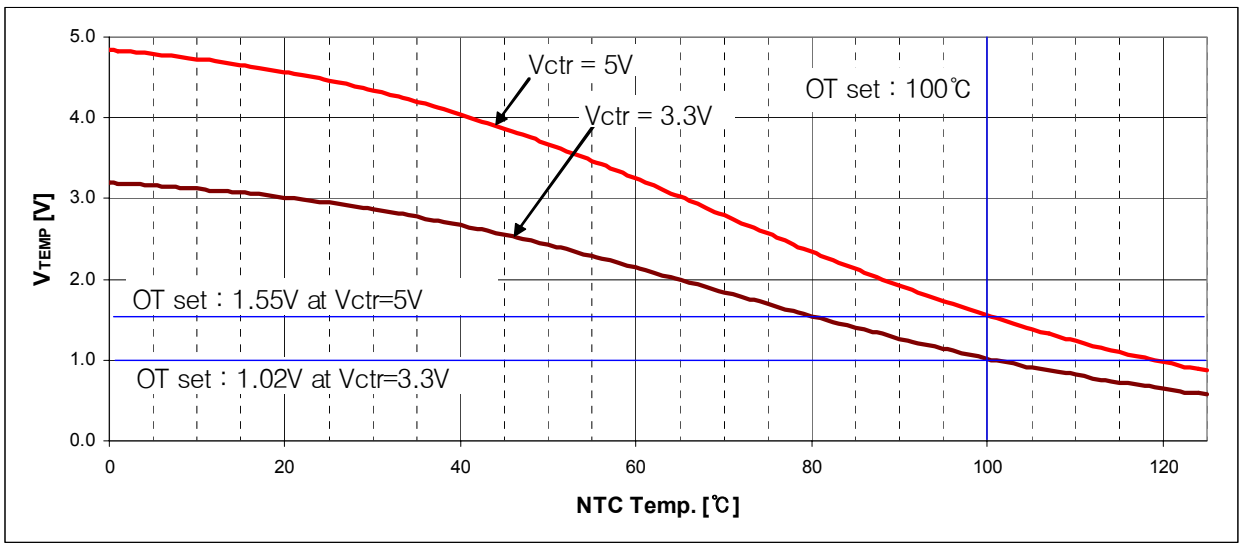

Figure 10 Voltage of /FLT_TEMP pin according to NTC temperature

As shown in **Figure 11**, when a voltage of /FLT_TEMP is decreased below OTP reference voltage 1.5$V_{typ.}$, single pulse of over $V_{IT,TH+}$ is generated at the ITRP input, and then CIPOS™ turns off all 6-IGBTs and fault-output is activated during typical 4.7ms(t_{FLTCLR}). So a voltage of /FLT_TEMP becomes low during fault-output duration time. However, It is noted that CIPOS™ operates normally after fault-output duration time, even though a voltage of /FLT_TEMP is still kept below OTP reference voltage. Therefore, for over temperature protection, it's necessary to be shut CIPOS™ down within single fault-output duration time by controller.

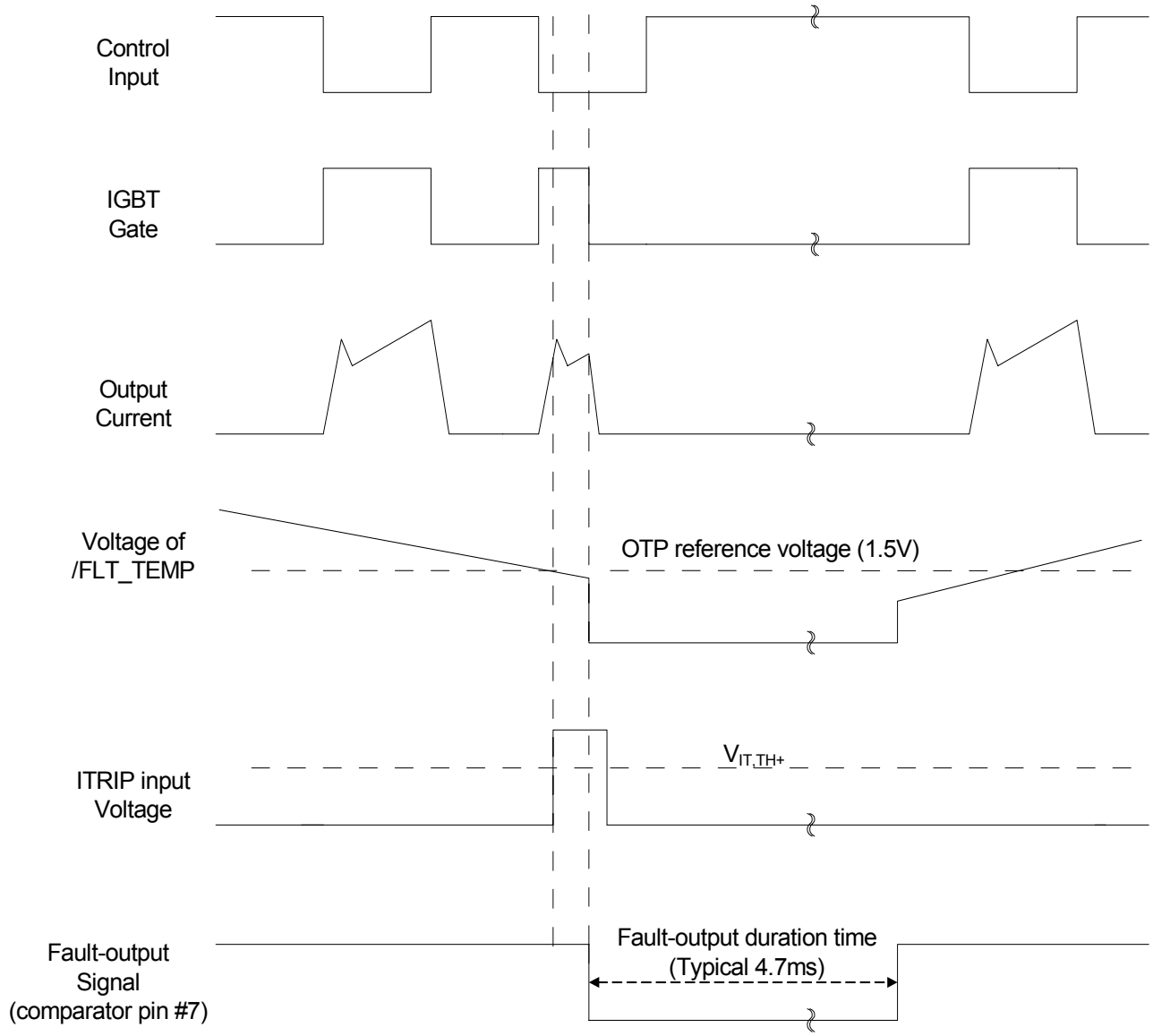

Figure 11 Timing chart of over temperature protection

5 Part List

Symbol	Components	Note
R1	1.8kΩ, 1/8W, 5%	Pull-up resistor for comparator output
R2	5.6kΩ, 1/8W, 1%	Voltage devider for reference voltage
R3	2.4kW, 1/8W, 1%	Voltage devider for reference voltage
R4	12kΩ, 1/8W, 1%	Voltage devider for reference voltage
R5	1.8kΩ, 1/8W, 5%	Pull-up resistor for comparator output ($\overline{Fo}$)
R6	3kΩ, 1/8W, 1%	Voltage devider for reference voltage
R7	5W, 5%	Current sensing resistor
R8	1.8kΩ, 1/8W, 5%	Series resistor for current sensing voltage
R9	12kΩ, 1/8W, 1%	Pull-up resistor for temperature sensing
C1	220uF 35V	+15V Bias voltage source capacitor
C2	1nF 25V	Series capacitor for single pulse at ITRIP
C3	1nF 25V	Bypass capacitor for reference voltage
C4	1nF 25V	Bypass capacitor for fault-output signal
C5	1nF 25V	Bypass capacitor for reference voltage
C6 ~ C8	4.7uF 35V	Bootstrap capacitors
C9	100uF 16V	+5V Bias voltage source capacitor
C10	10nF 25V	Bypass capacitor for +5V
C11	0.1uF 630V	Snubber capacitor
C12	1nF 25V	Bypass capacitor for current sensing voltage
C13	1nF 25V	Bypass capacitor for NTC temperature sensing
D1	1N4148	Diode for blocking current sensing voltage
D2	1N4148	Diode for discharging C2 capacitor
U1	LM393	Dual comparator for fault-output signal & OTP
U2	CIPOS™	Control Intergrated Power System
J1	12pin Connector	Signal & Power supply connector
U,V,W,P,N	Fasten Tap	Power terminals

6 PCB Design Guide

In general, there are several issues to be considered when designing a inverter board as below lists.

- Separate signal line and power line
- Low stray inductive connection
- Isolation distance
- Component placement

This chapter explains above considerations and method for the layout design.

6.1 Main Consideration of Layout Design

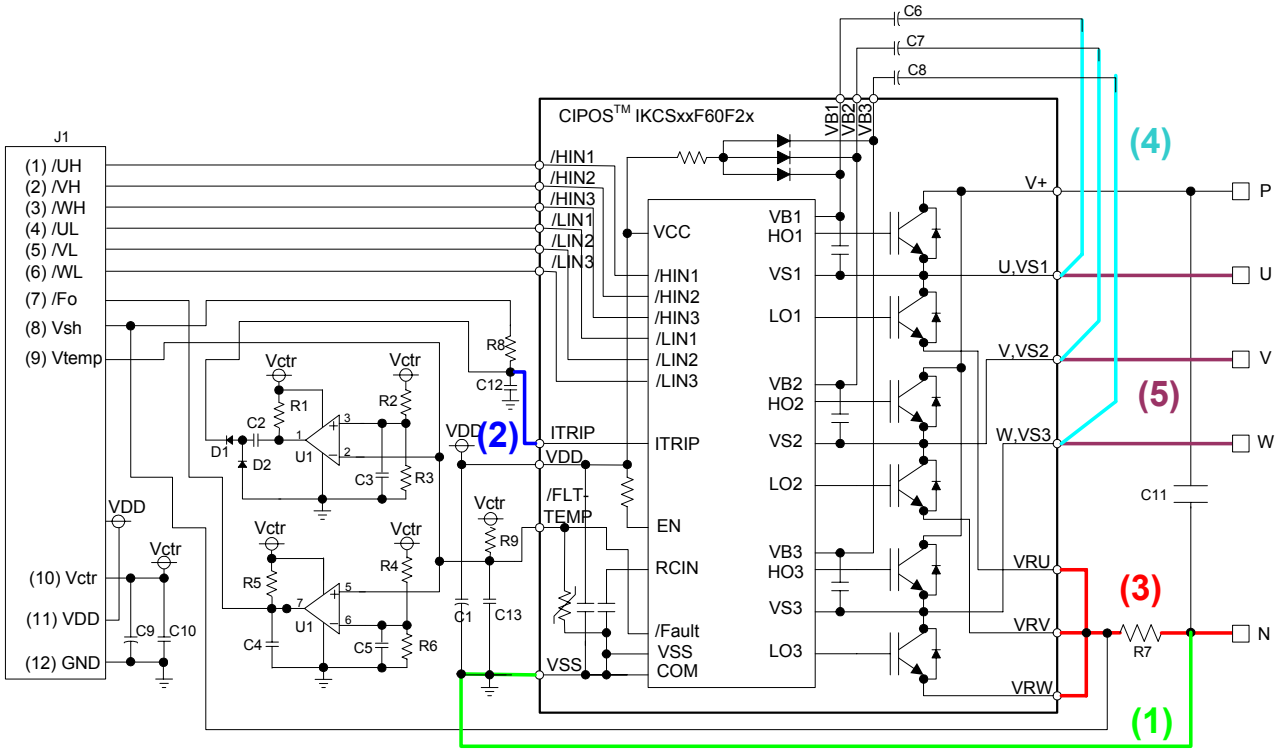

Figure 12 Example of interface circuit

Note.

1. (1)~(3) patterns should be as short as possible.
2. Signal GND(1) and Power GND(3) should be connected at only one point.
3. All of the bypass capacitors should be placed as close to the CIPOS™ as possible.
4. VS(4) and main output(5) patterns should be separated.
5. The snubber capacitor (C11) should be placed as close to the CIPOS™ as possible.

6.2 PCB Design Guide

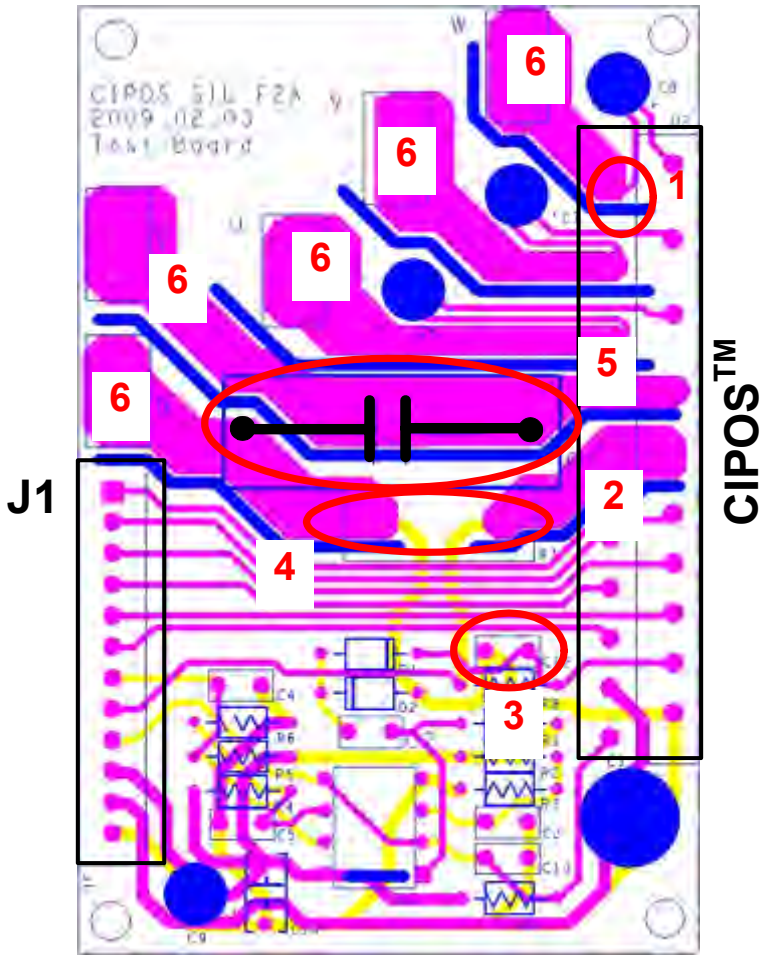

Figure 13 Example of PCB layout

Note.

1. Negative pin of bootstrap capacitor should be connected to output pin(U,V,W) directly and seperated from the main patterns of output.
2. The connection between 3 emitters of CIPOS™ (VRU,VRV,VRW) and shunt resistor should be as short and wide as possible to decrease stray inductance.
3. The capacitor for shunt voltage sensing should be placed as close to ITRIP pin as possible.
4. In order to detect the shunt voltage exactly, the sensing pattern of pink and the ground pattern of yellow should be wired from pin toward center of shunt resistor, and stretched out as shown in **Figure 13**.
5. The snubber capacitor should be placed as close to the terminals as possible.
6. The power patterns of U,V,W,P and N should be designed on both layer with vias to cover the high current and there should be kept the isolation distance among the power patterns over 2.5mm.

6.3 Layout of Reference Board

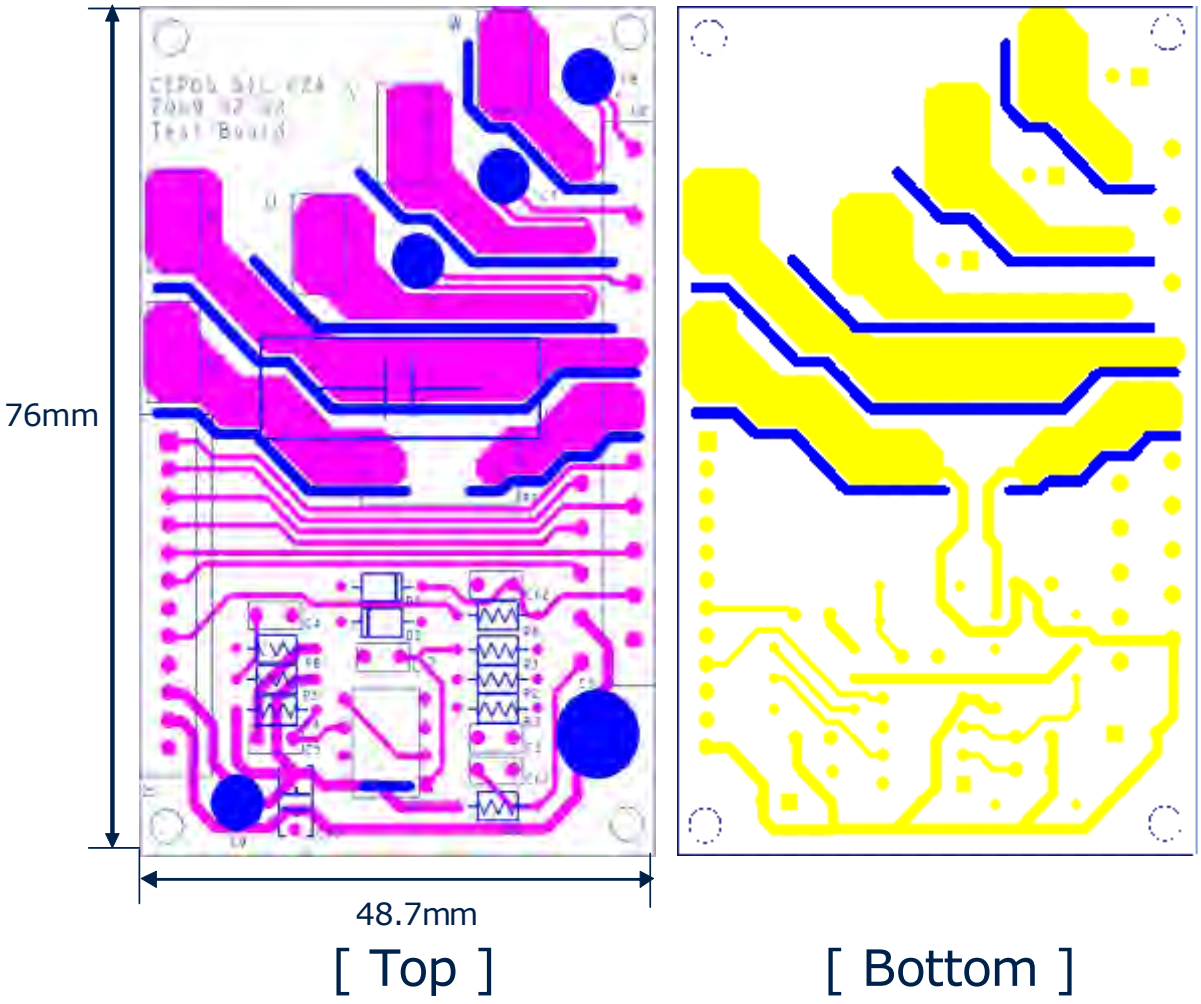

Figure 14 Layout of reference board for CIPOS™ IKCSxxF60F2A

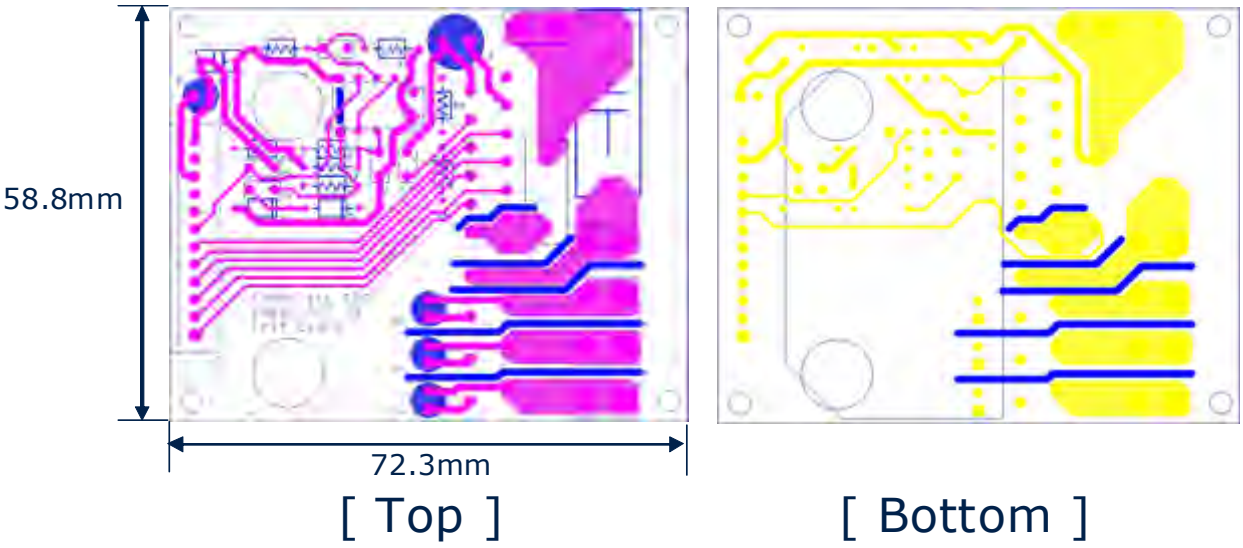

Figure 15 Layout of reference board for CIPOS™ IKCSxxF60F2C

Note.

1. All components except CIPOS™ IKCSxxF60F2C are placed on the top layer.
2. There are milling profiles in blue line to keep the isolation distance between power patterns, where the isolation distance is not enough.

7 Reference

[1] **Infineon Technologies:** CIPOS™ IKCS12F60F2A, IKCS12F60F2C; Preliminary Datasheet Rev. 2; Infineon Technologies, Germany, 2008.

[2] **Infineon Technologies:** CIPOS™ IKCSxxF60B(2)A - Reference Board for CIPOS™ SIL; Application Note V 1.0; Infineon Technologies, Korea, 2009