Control integrated Power System (CIPOS™)

Reference Board for CIPOS™ IKCSxxF60B(2)x

AN-CIPOS-Reference Board-2

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Power Management & Drives

Never stop thinking

Control integrated Power System (CIPOS™)
The Reference Board for CIPOS™ IKCSxxF60B(2)x

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1 Introduction

This reference board is composed of the CIPOS™ IKCSxxF60B(2)x, its minimum peripheral components and single shunt resistor. It is designed for customers to evaluate the performance of CIPOS™ with simple connection of the control signals and power wires.

The electrical circuit of both reference boards for IKCSxxF60B(2)A and IKCSxxF60B(2)C is exactly same, however, PCB layout of them is different due to the difference of lead forming type between IKCSxxF60B(2)A and IKCSxxF60B(2)C. **Figure 1** and **Figure 2** show the external view of two kinds of reference boards.

This application note describes how to design the key parameters and PCB layout.

Figure 1 The picture of a reference board for CIPOS™ IKCSxxF60B(2)A

Figure 2 The picture of a reference board for CIPOS™ IKCSxxF60B(2)C

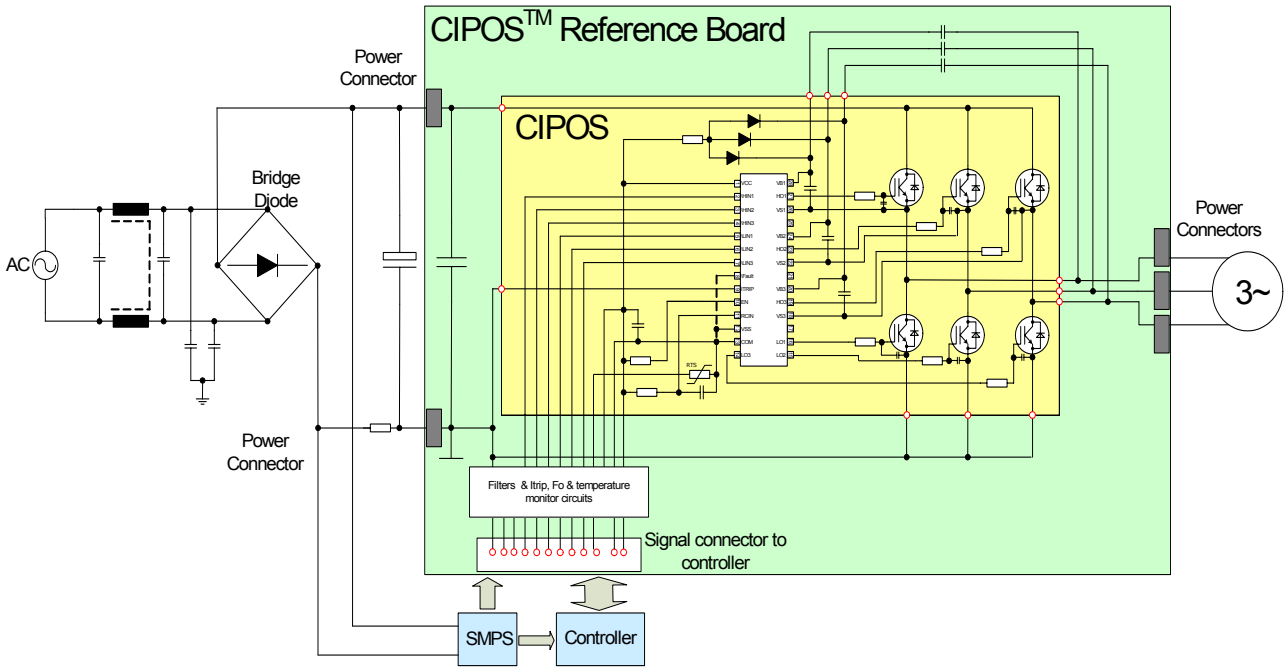

Figure 3 Application example

2 Schematic

Figure 4 shows a circuitry of the reference board for CIPOS™ IKCSxxF60B(2)x.

The reference board consists of interface circuit, bootstrap capacitors, snubber capacitor, short-circuit protection, over-temperature protection, fault output circuit and single shunt resistor. The CIPOS™ includes bypass capacitors of 100nF at each Vcc and VBS, so the external bypass capacitors are not necessary. And the internal bypass capacitors are located very close to the drive IC, thus this is good advantage to prevent malfunction by noise.

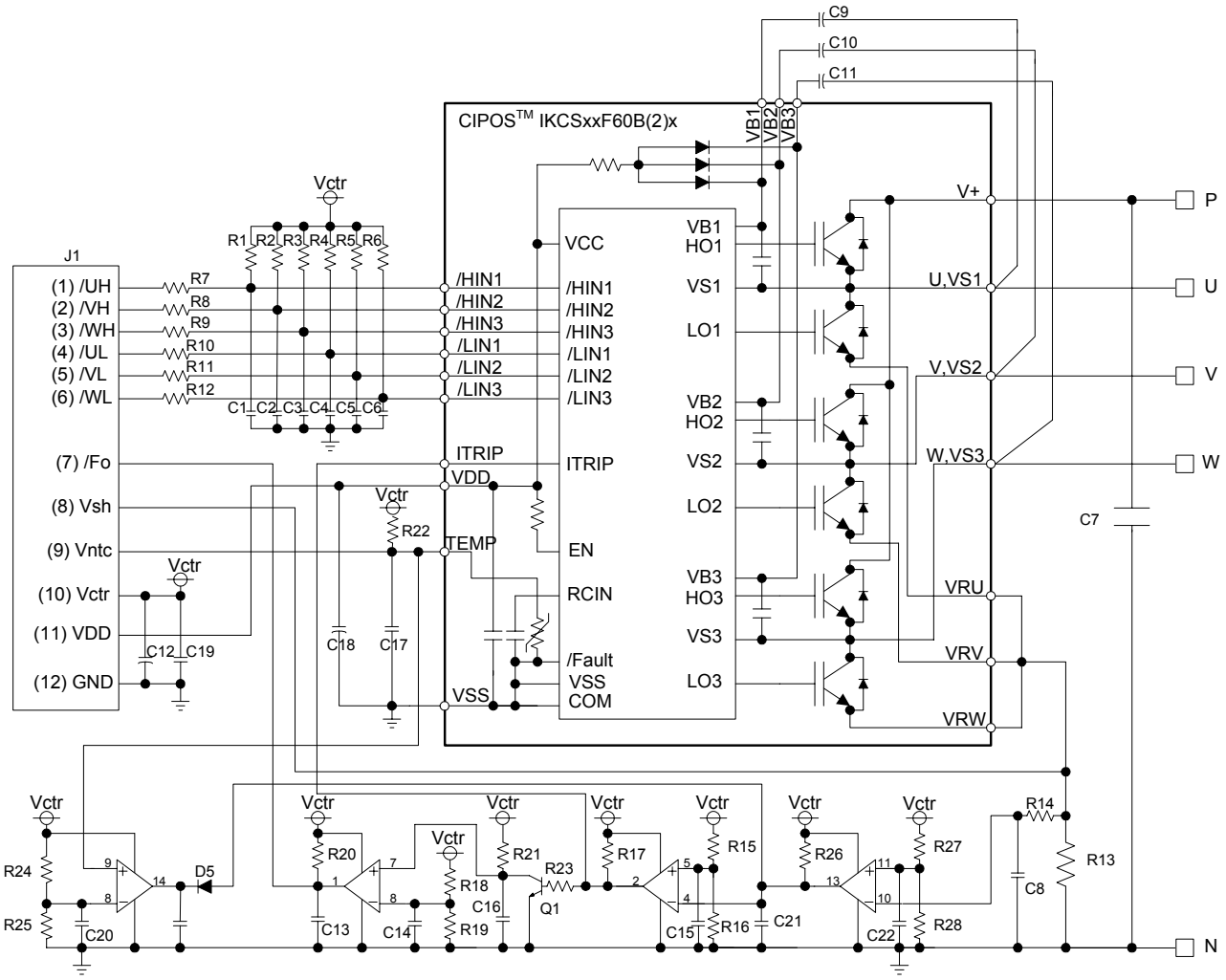

Figure 4 Circuit of the reference board

Note :

Vctr denotes the controller supply voltage such as 5V or 3.3V for MCU or DSP.

3 External Connection

3.1 Signal Connector (J1)

Pin	Name	Description
1	/UH	High side control signal input of U phase
2	/VH	High side control signal input of V phase
3	/WH	High side control signal input of W phase
4	/UL	Low side control signal input of U phase
5	/VL	Low side control signal input of V phase
6	/WL	Low side control signal input of W phase
7	/Fo	Fault output signal
8	Vsh	Shunt voltage sensing signal
9	Vtemp	Temperature sensing signal of CIPOS™
10	Vctr	External control voltage (5V or 3.3V)
11	VDD	External 15V supply voltage
12	GND	Ground

3.2 Power Connector

Pin	Description
U	Output terminal of U-phase
V	Output terminal of V-phase
W	Output terminal of W-phase
P	Positive terminal of DC-link voltage
N	Negative terminal of DC-link voltage

4 Key Parameters Design Guide

4.1 Circuit of Input Signals ($\overline{\text{LIN}}$, $\overline{\text{HIN}}$)

The input signals can be either TTL- or CMOS-compatible. The logic levels can go down to 3.3V. The maximum input voltage of the pins is internally clamped to 10.5 V. However, the recommended voltage range of input voltage is up to 5V. The control pins LIN and HIN are active low.

They all have an internal pull-up structure with a pull-up resistor value of nominal 75 kΩ. The integrated pull-up resistors are designed to pull up the internal structures, so that the IC can control CIPOS™ safely. For the more stable operation, an external pull-up circuit is necessary and recommended value is under 4.7kΩ.

The input noise filter inside CIPOS™ suppresses short pulse and prevents the driven IGBT from excessive switching loss. The input noise filter time is typically 270ns. This means that an input signal must stay on its level for this period of time in order that the state change is processed correctly.

And as shown in **Figure 5**, R of 100Ω and C of 1nF for the RC filter of interface circuit is recommended in order to operate safely in harsh environment in terms of EMI. Please place RC-filter as close to the input pins of CIPOS™ as possible.

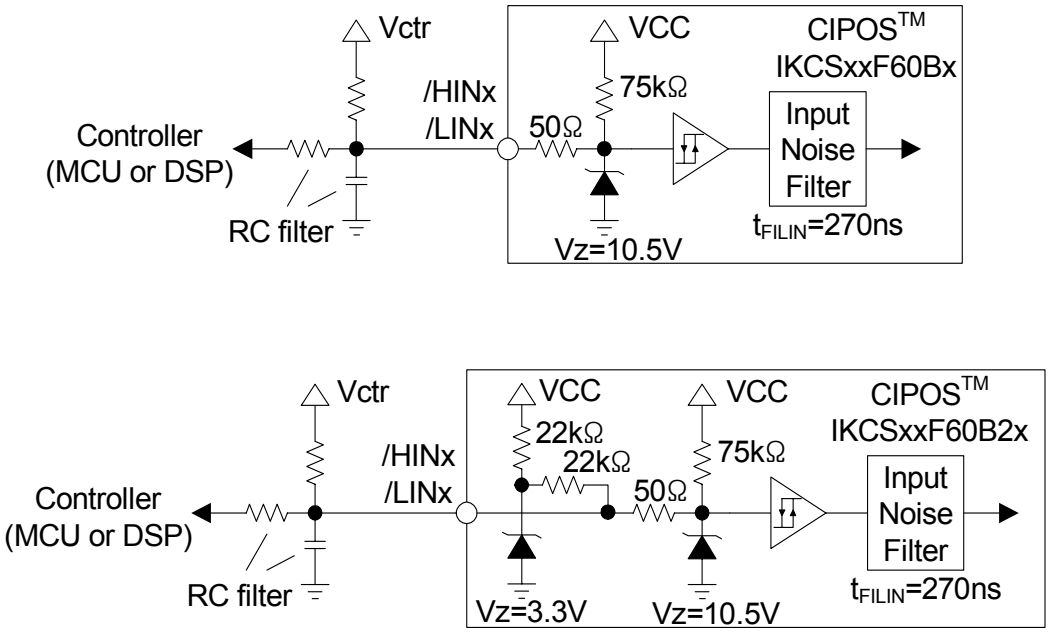

Figure 5 RC-filter of input signals and pull-up circuit

4.2 Bootstrap Capacitor

Bootstrapping is a common method of pumping charges from a low potential to a higher one. With this technique a supply voltage for the floating high side sections of the gate drive can be easily established according to **Figure 6**. It is only the effective circuit shown for one of the three half bridges. The bootstrap resistor R_{BS} is connected to each of the three bootstrap diodes in the module to limit current. Please refer to the datasheet and application note for the internal circuit and bootstrapping method in detail.

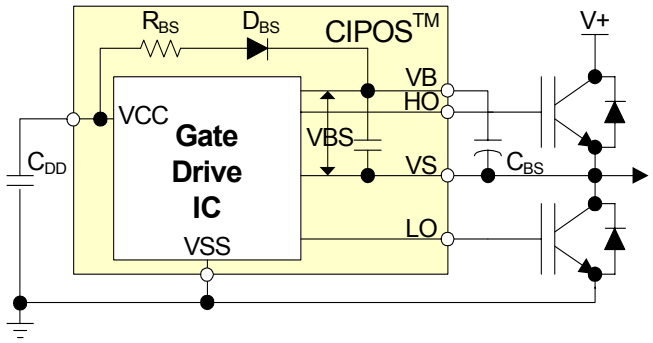

Figure 6 Bootstrap circuit for the supply of a high side gate drive

A low leakage current of the high side section is very important in order to keep the bootstrap capacitors small. The C_{BS} discharges mainly by the following machanisms:

- Quiescent current to the high side circuit in the IC
- Gate charge for turning high side IGBT on
- Level-shift charge required by level shifters in the IC
- Leakage current in the bootstrap diode
- C_{BS} capacitor leakage current (ignored for non-electrolytic capacitor)
- Bootstrap diode reverse recovery charge

The calculation of the bootstrap capacitor results in

$$C_{BS} = \frac{I_{leak} \times t_p}{\Delta v_{BS}}$$

with I_{leak} being the maximum discharge current of C_{BS}, t_P the maximum on pulse width of high side IGBT and Δv_{BS} the voltage drop at the bootstrap capacitor within a switching period.

Practically, the recommended leakage current is 1mA of I_{leak} for CIPOS™.

Figure 7 shows the curve corresponding to above equation for a continuous sinusoidal modulation, if the voltage ripple Δv_{BS} is 0.1V. The recommended bootstrap capacitance for a continuous sinusoidal modulation method is therefore in the range up to 4.7µF for most switching frequencies. In other pwm method case like a discontinuous sinusoidal modulation, tp must be set the longest period of the low side IGBT off.

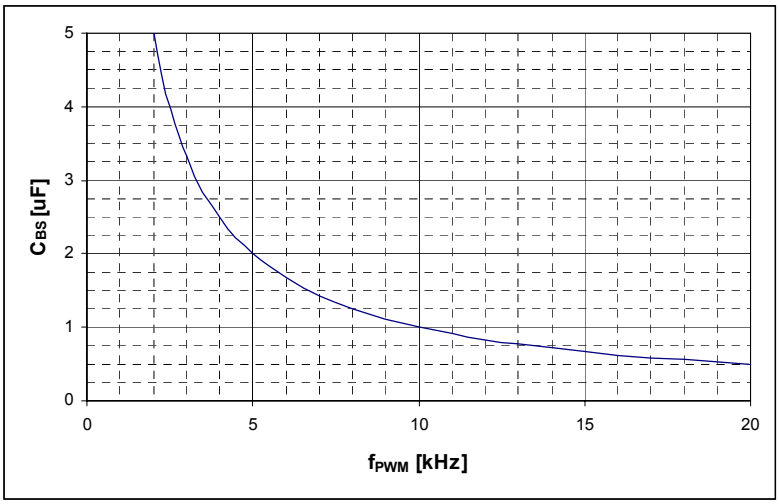

Figure 7 Size of the bootstrap capacitor as a function of the switching frequency f_{PWM}

4.3 Short-Circuit Protection

The reference board has a comparator circuit for the short-circuit (SC) protection and fault output signal. The SC protection level is decided by reference voltage in negative input of comparator and comparator output is connected to Itrip pin of CIPOS™. Please refer to **Figure 8** for a detail circuit of SC protection.

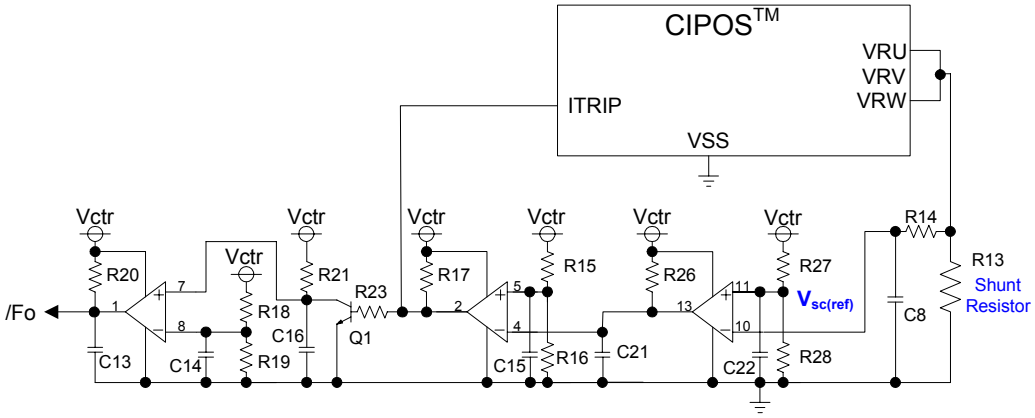

Figure 8 Short-circuit protection circuit

4.3.1 Shunt Resistor Selection

The value of shunt resistor is calculated by the following equation.

$$R_{SH} = \frac{V_{SC(ref)}}{I_{SC}}$$

Where $V_{SC(ref)}$ is the SC reference voltage of comparator negative input and I_{SC} is the current of SC detection level.

In the **Figure 8**, $V_{SC(ref)}$ is determined by voltage divider(R27, R28). For example, when the control voltage Vctr is 5V, R27=10kΩ and R28=1kΩ then $V_{SC(ref)}$ is $0.45V_{typ.}$. The SC reference voltage should be selected according to the application and user's demand. The resistor for voltage divider should be a precision resistor such as 1% to decrease tolerance.

The maximum value of SC protection level should be set less than the repetitive peak collector current in the datasheet considering the tolerance of shunt resistor.

For example, the maximum peak collector current of IKCS12F60B(2)A is $18A_{peak}$,

$$R_{SH(min)} = 0.45 / 18 = 0.025\Omega$$

So the recommended value of shunt resistor is over 25mΩ for IKCS12F60B(2)A.

For the power rating of the shunt resistor, the below lists should be considered.

- Maximum load current of inverter (I_{rms})
- Shunt resistor value at Tc=25°C (R_{SH})
- Power derating ratio of shunt resistor at T_{SH}=100°C
- Safety margin

And the power rating is calculated by following equation.

$$P_{SH} = \frac{I_{rms}^2 R_{SH} \times margin}{Derating\ ratio}$$

For example, In case of IKCS12F60B(2)A and R_{SH}=25mΩ

- Max. load current of inverter : $6A_{rms}$
- Power derating ratio of shunt resistor at T_{SH}=100°C : 80%
- Safety margin : 30%

$$P_{SH} = \frac{6^2 \times 0.025 \times 1.3}{0.8} = 1.46W$$

So the proper power rating of shunt resistor is over 2W.

Based on the previous equations, conditions, and calaulation method, minimum shunt resistance and resistor power according to all kinds of CIPOS™ IKCSxxF60xxx products are introduced as shown in below table.

It's noted that a proper resistance and its power over than minimum values should be chosen considering over-current protection level required in the application set.

Products	Maximum Peak Current	**Minimum** shunt resistance, $\mathbf{R_{SH}}$	**Minimum** shunt resistor power, $\mathbf{P_{SH}}$
IKCS22F60x(2)x	45	10mΩ	4W
IKCS17F60x(2)x	30	15mΩ	3W
IKCS12F60x(2)x	18	25mΩ	2W
IKCS08F60x(2)x	12	38mΩ	1W

4.3.2 Delay Time

The RC filter should be necessary in SC sensing circuit to prevent malfunction of SC protection due to noise interference. The RC time constant is determined by applying time of noise and the withstand time capability of IGBT.

When the current on shunt resistor exceeds SC protection level(I_{sc}), this voltage is applied to the positive input pin of comparator via the RC filter. The filter delay time(t1) that the positive input voltage of comparator rises to the SC reference voltage is caused by RC filter time constant.

In addition there are the response time of comparator(t2), Input filter time of Itrip(t3) and shutdown propagation delay of Itrip(t4). Please refer to the below table.

Item	min.	typ.	max.	unit
Response time of comparator (t2)	-	300	-	ns
Input filter time of Itrip (t3)	155	225	380	ns
Shutdown propagation delay (t4)	-	900	-	ns

Therefore, the total delay time from occurrence of SC to shutdown of the IGBT gate becomes

$$t_{Total} = 2xt1 + t2 + t3 + t4$$

The total delay should be less than 5us of short circuit withstand time(t_{SC}) in datasheet. Thus, RC time constant should be set in the range of 1~2us. It is recommended that R of 1.8kΩ and C of 1nF.

4.4 External Fault-Output Duration Time

If the Itrip pin voltage of CIPOS™ exceeds the positive threshold voltage of Itrip $V_{IT,TH+}$, then CIPOS™ turns off all 6-IGBTs during 4ms(t_{FLTCLR}). So the output of comparator(/Fo) should be kept low over 4ms and the controller should be off state after the fault signal is detected. An external fault-output duration time is over 5ms by RC time constant of R21 and C16, where the control supply voltage Vctr is 5V or 3.3V, R21 is 510kΩ and C16 is 10nF. It can be also cotrolled by changing the resistance and capacitance which are connected to the comparator negative input.

Please refer to **Figure 8** for the circuit and **Figure 9** for the timing chart of SC protection.

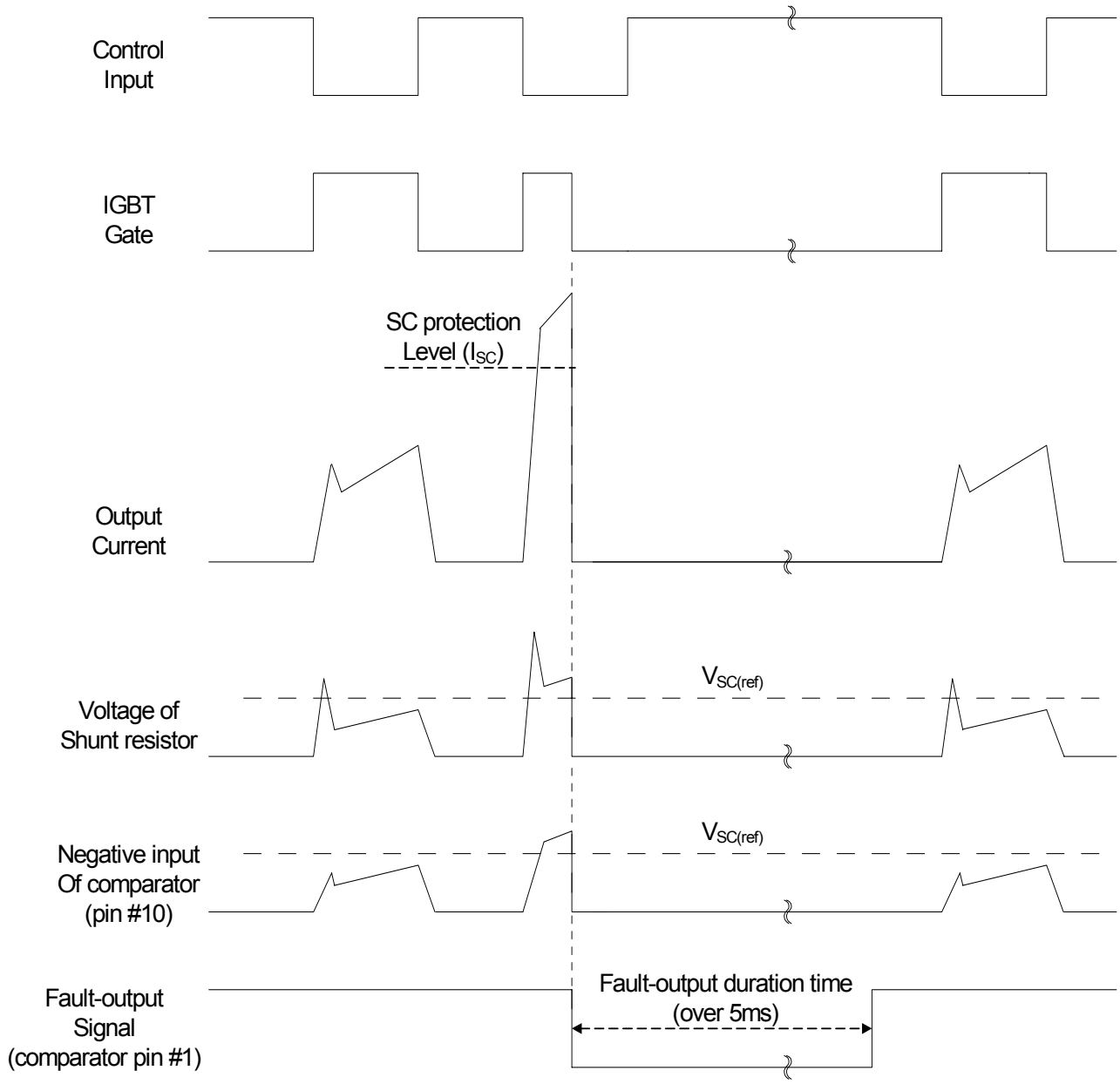

Figure 9 Timing chart of SC protection

4.5 Over-Temperature Protection

The CIPOS™ includes NTC of 100kΩ at 25°C. The NTC should be pulled up to 5V or 3.3V with external resistor (R22), and V_{TEMP} is determined by voltage divider (R24, R25). For example, when the control voltage Vctr is 5V or 3.3V, R22=20kΩ , R24=7.5kΩ and R25=2kΩ , then V_{TEMP} at 100°C of NTC temperature is 1.06$V_{typ.}$ at Vctr=5V and 0.7V at Vctr=3.3V, and the set level of over-temperature protection at NTC is about 100°C as shown in **Figure 10** and **Figure 11**.

After over temperature protection is set, operating mechanism of this function is same as short-circuit protection like fault out and internal 6 IGBTs shut down. Therefore, please refer to the chapter 4.3.

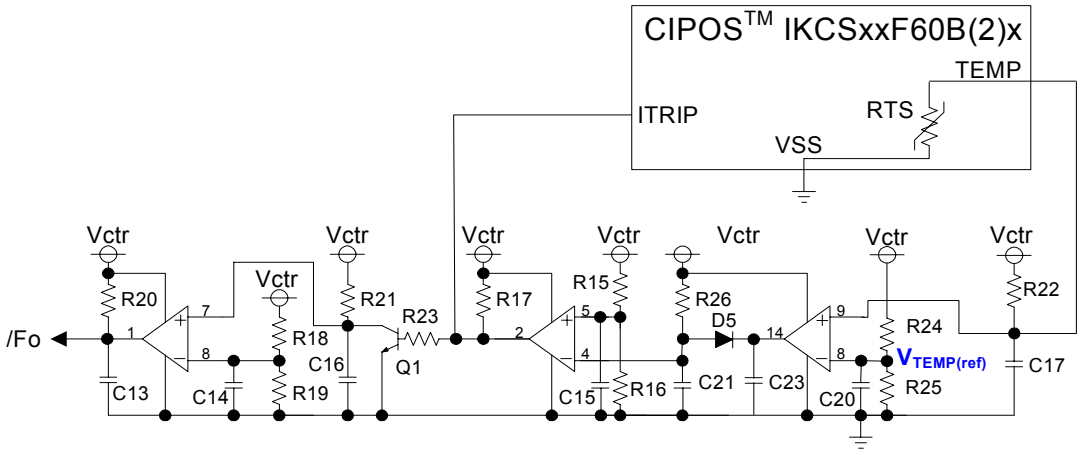

Figure 10 Over-temperature protection with NTC

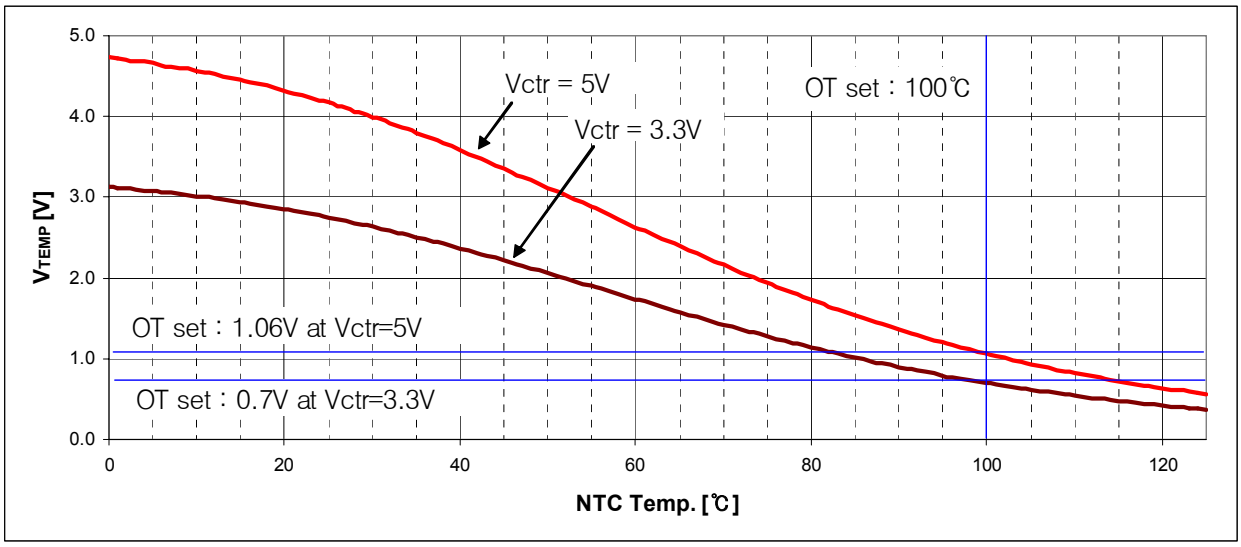

Figure 11 Voltage of TEMP pin according to the NTC temperature

5 Part List

Symbol	Components	Note
R1~R6	4.7kΩ, 1/8W, 5%	Pull-up resistors for input signal
R7~R12	100Ω, 1/8W, 5%	Series resistors for input signal
R13	5W, 5%	Current sensing resistor
R14	1.8kΩ, 1/8W, 5%	Series resistor for current sensing voltage
R15	1kΩ, 1/8W, 1%	Voltage devider for reference voltage
R16	3.9kΩ, 1/8W, 1%	Voltage devider for reference voltage
R17	3.9kΩ, 1/8W, 5%	Pull-up resistor for Comparator Output (V_{Itrip})
R18	10kΩ, 1/8W, 1%	Voltage devider for reference voltage
R19	20kΩ, 1/8W, 1%	Voltage devider for reference voltage
R20	2kΩ, 1/8W, 5%	Pull-up resistor for comparator output ($\overline{Fo}$)
R21	510kΩ, 1/8W, 5%	Pull-up resistor for comparator input ($\overline{Fo}$)
R22	20kΩ, 1/8W, 1%	Pull-up resistor for temperature sensing
R23	1kΩ, 1/8W, 5%	Base resistor of PNP transistor
R24	7.5kΩ, 1/8W, 5%	Voltage devider for V_{TEMP}
R25	2kΩ, 1/8W, 5%	Voltage devider for V_{TEMP}
R26	4.7kΩ, 1/8W, 5%	Pull-up resistor for comparator output
R27	10kΩ, 1/8W, 5%	Voltage devider for $V_{SC(ref)}$
R28	1kΩ, 1/8W, 5%	Voltage devider for $V_{SC(ref)}$
C1~C6	1nF 25V	Bypass capacitors for input signal
C7	0.1uF 630V	Snubber capacitor
C8	1nF 50V	Bypass capacitor for current sensing voltage
C9~C11	4.7uF 35V	Bootstrap capacitors
C12	100uF 16V	+5V Bias voltage source capacitor
C13	100pF 25V	Bypass capacitor for fault-output signal
C14,C15	100nF 25V	Bypass capacitors for reference voltage
C16	10nF 25V	Bypass capacitor for $\overline{Fo}$ duration time
C17	100nF 25V	Bypass capacitor for NTC temperature sensing
C18	220uF 35V	+15V Bias voltage source capacitor
C19	100nF 25V	Bypass capacitor for +5V
C20	100nF 25V	Bypass capacitor for reference voltage
C21	1nF 25V	Bypass capacitor for comparator output

C22	100nF 25V	Bypass capacitor for reference voltage
C23	1000nF 25V	Bypass capacitor for signal stable of comparator output
D5	1N4148	Diode for blocking C23 voltage
U1	CIPOS™	Control Intergrated Power System
U2	LM2901N	Quad comparator for fault-output signal
Q1	2N2222	PNP transistor
J1	12pin Connector	Signal & Power supply connector
U,V,W,P,N	Fasten Tap	Power terminals

6 PCB Design Guide

In general, there are several issues to be considered when designing a inverter board as below lists.

- Separate signal line and power line
- Low stray inductive connection
- Isolation distance
- Component placement

This chapter explains above considerations and method for the layout design.

6.1 Main Consideration of Layout Design

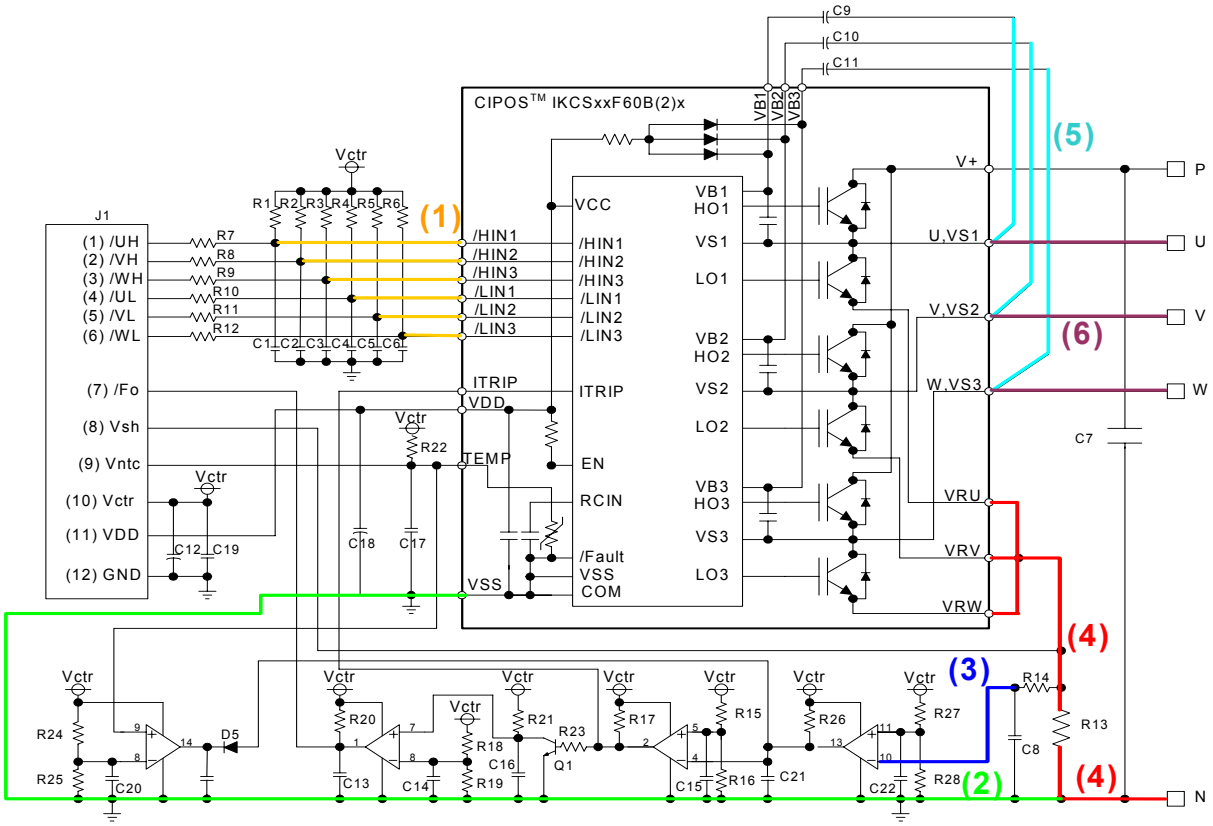

Figure 12 Example of Interface Circuit

Note.

1. (1)~(4) patterns should be as short as possible.
2. Signal GND(2) and Power GND(4) should be connected at only one point.
3. All of the bypass capacitors should be placed as close to the CIPOS™ as possible.
4. VS(5) and main output(6) patterns should be separated.
5. The snubber capacitor (C7) should be placed as close to the CIPOS™ as possible.

6.2 PCB Design Guide

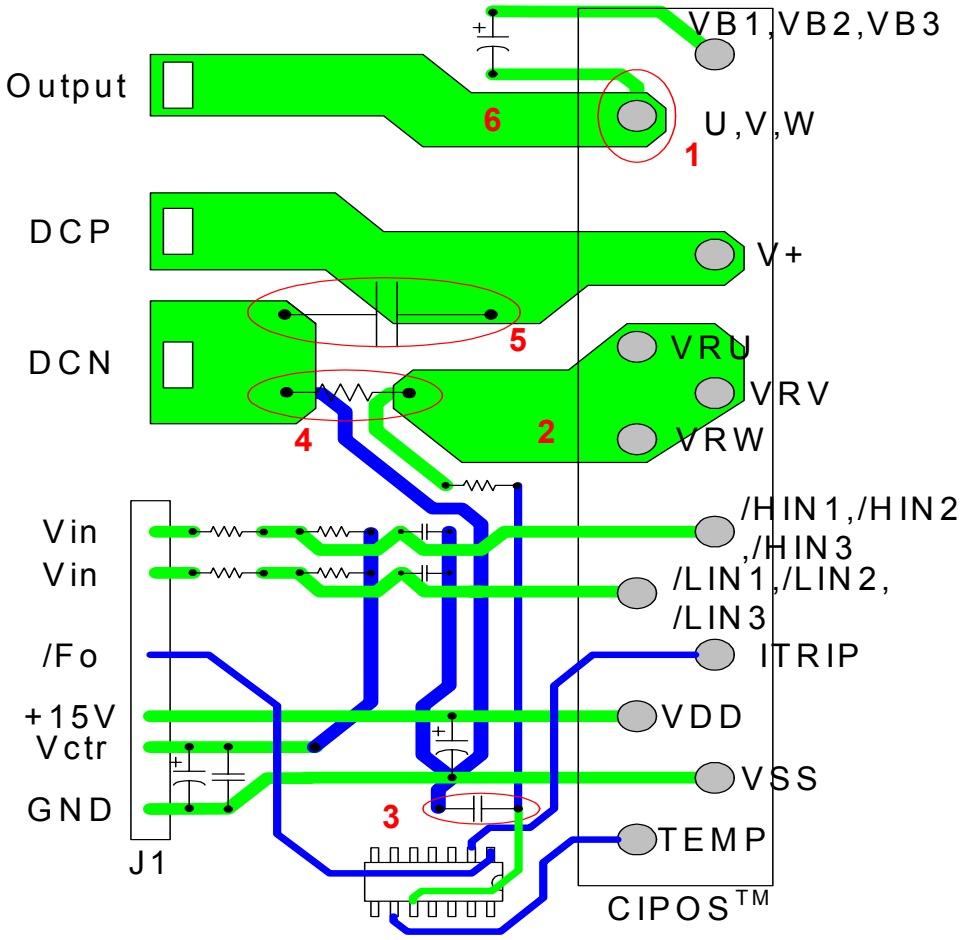

Figure 13 Example of PCB Layout

Note.

1. Negative pin of bootstrap capacitor should be connected to output pin(U,V,W) directly and seperated from the main patterns of output.
2. The connection between 3 emitters of CIPOS™ (VRU,VRV,VRW) and shunt resistor should be as short and wide as possible to decrease stray inductance.
3. The capacitor for shunt voltage sensing should be placed as close to comparator as possible.
4. In order to detect the shunt voltage exactly, the sensing pattern of green and the ground pattern of blue should be wired from pin toward center of shunt resistor, and stretched out as shown in **Figure 13**.
5. The snubber capacitor should be placed as close to the terminals as possible.
6. The power patterns of U,V,W,P and N should be designed on both layer with vias to cover the high current and there should be kept the isolation distance among the power patterns over 2.5mm.

6.3 Layout of The Reference Board

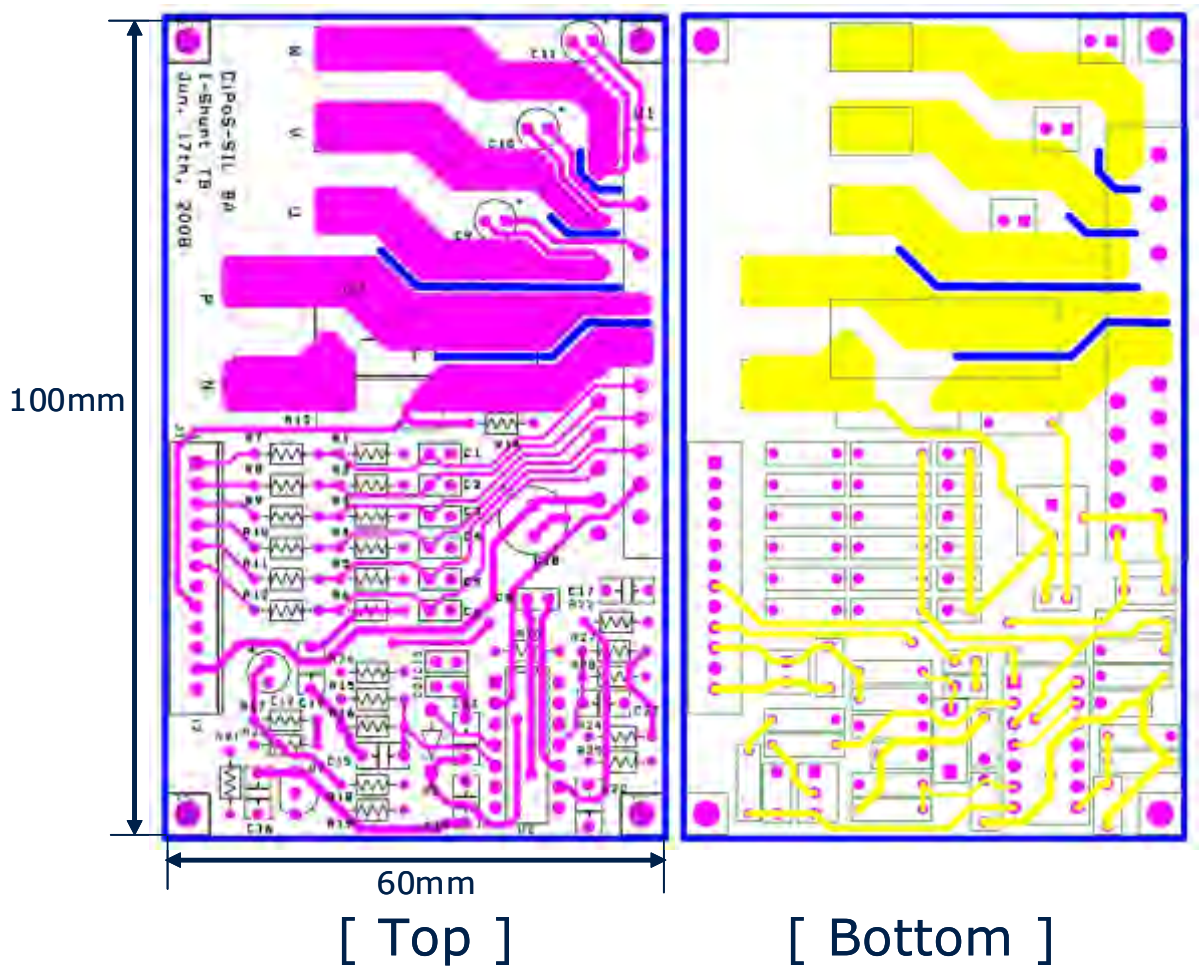

Figure 14 Layout of The Reference Board for CIPOS™ IKCSxxF60B(2)A

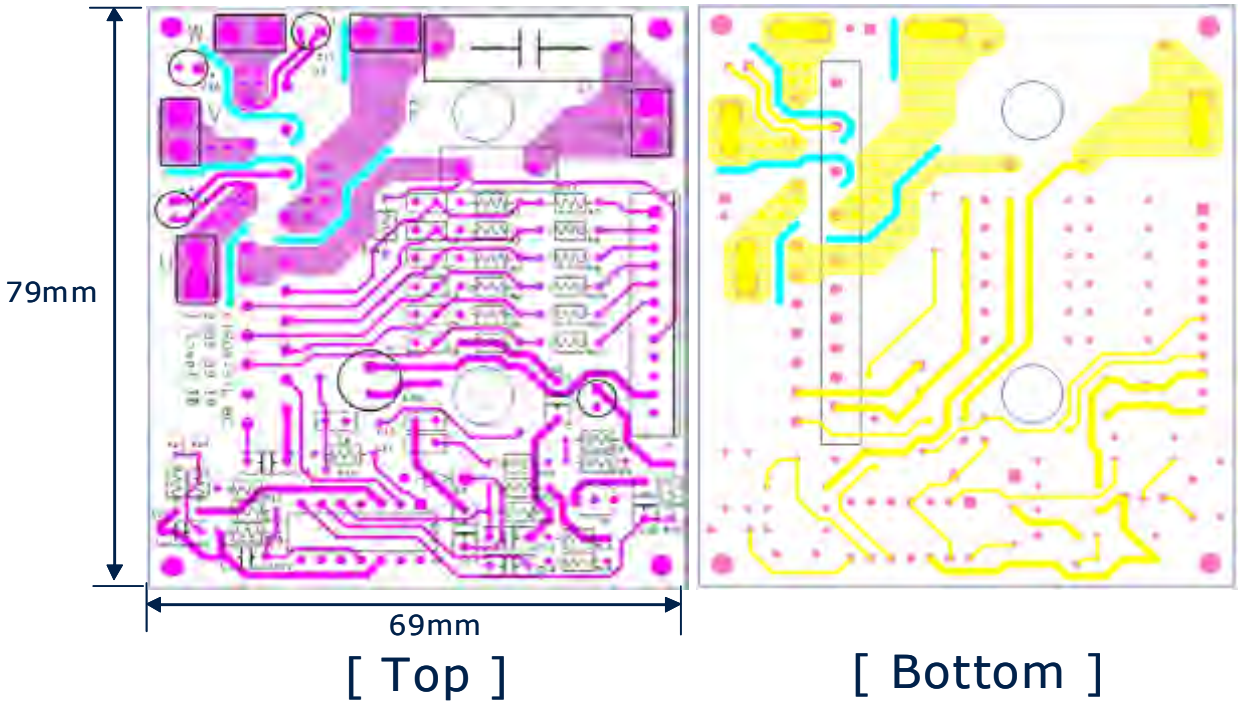

Figure 15 Layout of The Reference Board for CIPOS™ IKCSxxF60B(2)C

Note.

1. All components except CIPOS™ IKCSxxF60B(2)C are placed on the top layer.
2. There are milling profiles in blue line to keep the isolation distance between power patterns, where the isolation distance is not enough.

7 Reference

[1] **Infineon Technologies:** CIPOS™ IKCS12F60BA, IKCS12F60BC, IKCS08F60B2A; Preliminary Datasheet Rev. 2; Infineon Technologies, Germany, 2008.

[2] **Infineon Technologies:** CIPOS™ IKCS12F60AA - The Reference Board for CIPOS™ SIL AA; Application Note V 2.0; Infineon Technologies, Korea, 2008