

Control integrated Power System (CIPOSTM)

CIPOSTM Control Input Interface
Compatibility for 3.3V / 5V
Microcontroller

DN-CIPOS-2

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<http://www.infineon.com/cipos>

Power Management and Drives



Never stop thinking

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1 Introduction

The control inputs HINx and LINx of the CIPOS™ are low active. In order to ensure that all outputs are low if the inputs are in the floating state (open or tri-state), there is a internal pull-up resistor to V_{cc} for every input pin as shown in the figure 1. As specified in the datasheet, the input clamp voltage of the control inputs HINx/LINx is 10.1V typically @ I_{IN} = 4mA.

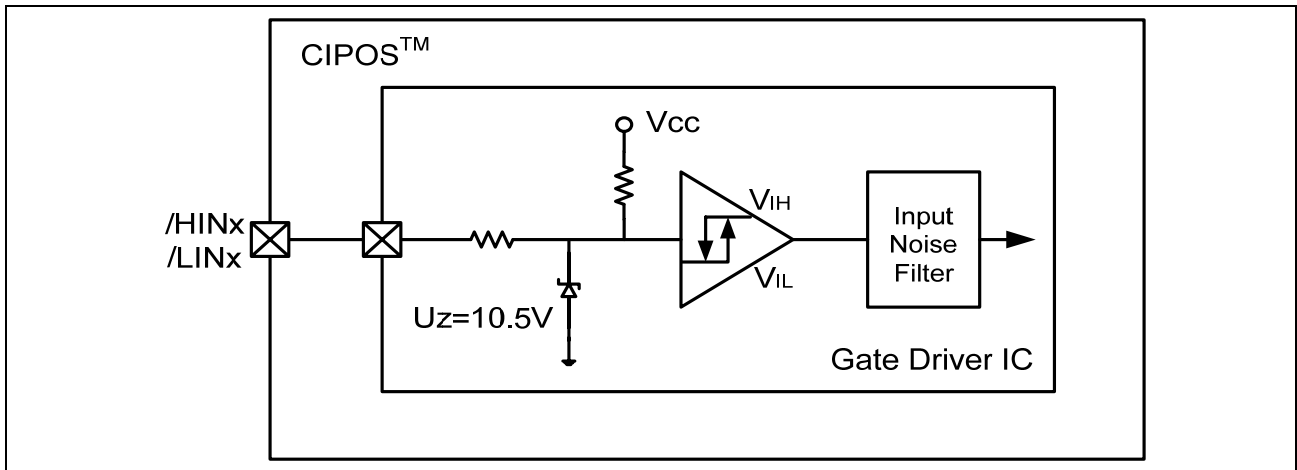


Figure 1 The internal circuit of the CIPOS™ control input pin HINx/LINx

This high clamp voltage may be critical for some 3.3V / 5V microcontrollers because it causes current flowing from CIPOS™ control inputs into the connected microcontroller outputs, which may damage the output clamping stage or ESD structure of some microcontrollers. The current, which may be drawn out of the control inputs of CIPOS™ during tri-state of the microcontroller, is maximum 100µA. Any ESD structure of microcontrollers should be stable against this stress continuously. However, it is recommended to contact the microcontroller manufacturer for a confirmation. Besides, the further consideration to the interface compatibility is necessary for some microcontrollers.

2 Interface compatibility for CIPOS™ Control Inputs

To archive a interface compatibility for 3.3V / 5V microcontrollers with CIPOS™ standard products (IKCSxxF60Ax/Bx/Dx), an external pull-up circuit is recommended as shown in the figure 2. This is a standard design rule for a good designed and reliable interface from CIPOS™ to any microcontroller.

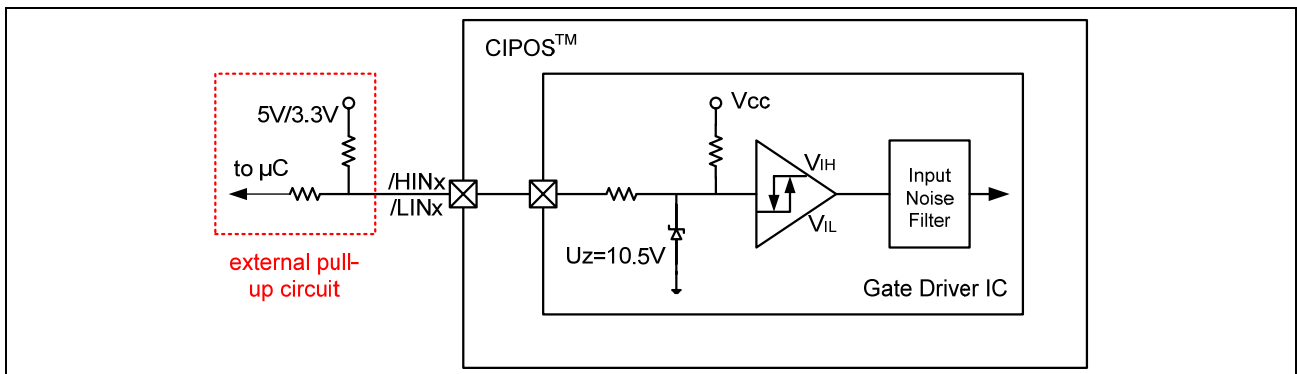


Figure 2 External Pull-up Circuit for the Standard CIPOS™ Products

If the external pull-up circuit is not preferred, CIPOS™ also provides a special series (IKCSxxF60B2x) with internal additional clamp structure to clamp the control inputs of CIPOS™ under 4.2V. This internal clamp structure is shown in the figure-3: an additional zener diode is used to achieve the reduction of the clamp voltage.

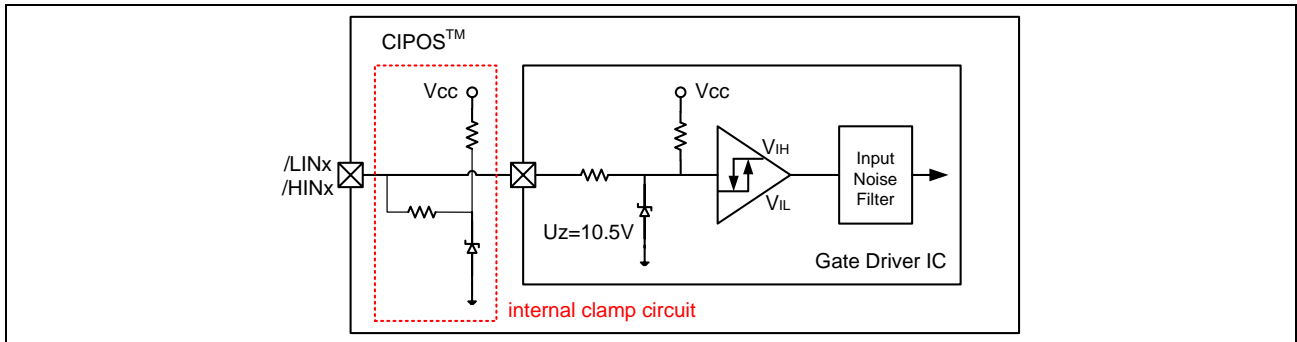


Figure 3 Internal clamp structure in CIPOS™ B2x Version

The reduced clamp voltage (pins open) measured at different V_{cc} is given in the table 1.

Table 1 HINx/LINx clamp voltage @ different V_{cc}

V_{cc}	HINx/LINx (typical)
20V	4.2V
15V	4.1V
9.5V	3.7V

3 Conclusion

The clamp structure for control input pins HINx/LINx inside CIPOS™ ensures a safe switch off behavior nevertheless which could damage the microcontroller output stage. To solve this potential problem, an external pull-up circuit is recommended for CIPOS™ in the system application design.

CIPOS™ also provides B2x series for an additional internal clamp solution to reduce the voltage at HINx/LINx pins under 4.1V typically (pin open or in tri-state), if the external pull-up circuit is not preferred.

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