Control integrated Power System (CIPOS™)

IKCS12F60AA - Technical Description

AN-CIPOS-1

Authors: Wolfgang Frank

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Power Management & Drives

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IKCS12F60AA - Technical Description

Revision History: 2008-03 V1.1

Previous Version:

Page	Subjects (major changes since last revision)
	extended section of bootstrapping

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Edition 2008-03

Published by
Infineon Technologies AG
81726 München, Germany

1 Short Description

The Control integrated Power System (CIPOS™) is a molded module, which contains all necessary power and gate drive components for setting up a speed variable electric drive according to **Figure 1**. This application note describes particularly the devices IKCS12F60AA and IKCS12F60AB. CIPOS™ is a ready to use solution for all drive systems up to a power rating of P_{out} = 1 kW and is designed for application in consumer drives such as washing machines and air conditioners. Many of the design hints are also valid for other devices.

Please refer to the application note “AN-Gatedrive-6ED003-1” for further information concerning the gate drive IC.

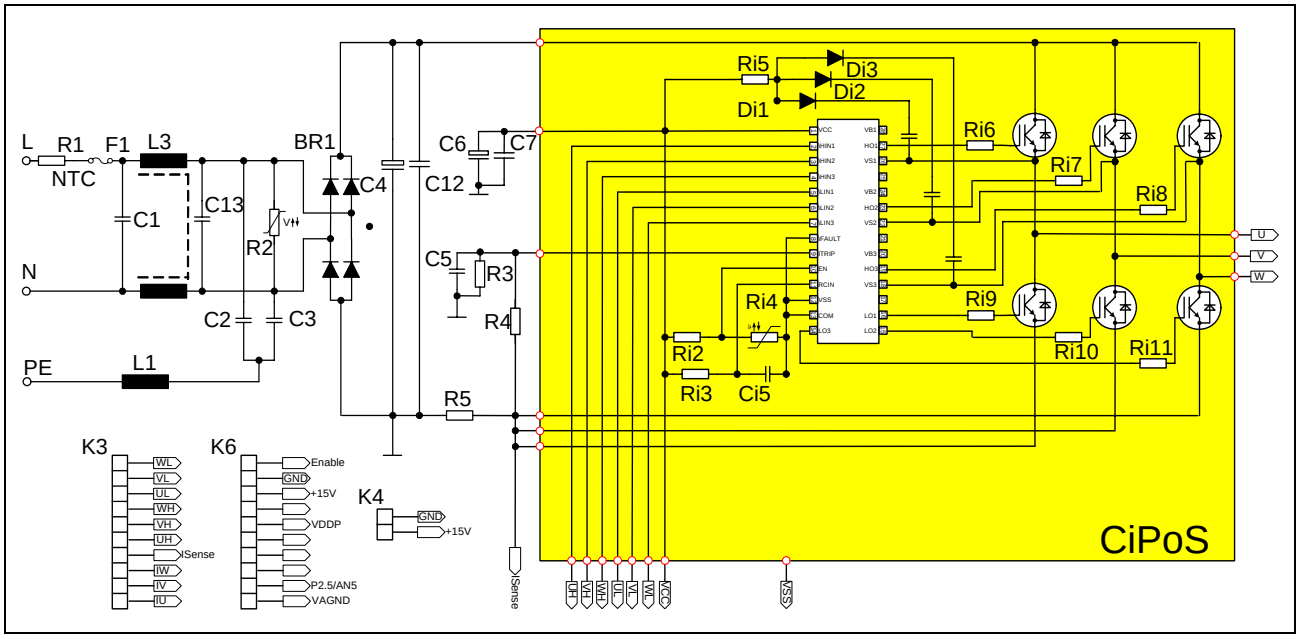

Figure 1 Typical Application of CIPOS™

2 Package Technology

Figure 2 shows a transparent picture of the CIPOS™ package. Inside the package there is a DCB substrate. It contains all the power components such as the diodes and the IGBT and isolates them from each other and from the heatsink. It is important to note, that this material provides also very low thermal resistance as it is explained more detailed in **Section 2.1**.

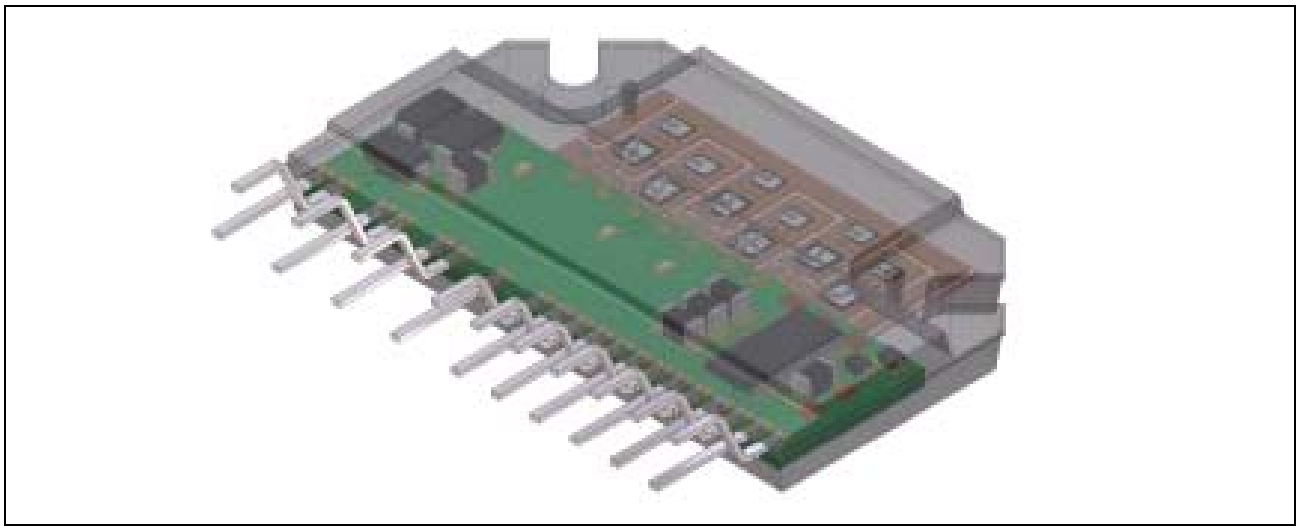

Figure 2 Insight view into the CIPOS™ package

All the low power components such as the gate drive IC, the gate resistors or the bootstrap circuit are assembled on a PCB. PCB technology allow a very easy routing with EDA tools as they are commonly available.

The mold process is considered for having a solid contact to the PCB and the DCB, so that the only measure in terms of blocking voltage is the voltage withstand capability of the mold compound itself. No further creepage distances are important inside the package, so that routing rules and component placement rules must not be considered. Please refer to **Section 2.2** for the creepage distances and related topics.

2.1 Thermal Capabilities and DC Current Rating

The advantage of this material is its low thermal resistance, so that thermal resistances junctio to case of R_{thJCI} =3.0 K/W f or the IGBT and R_{thJCD} =4.1K/W for the diode are possible.

This leads to a significantly lower cost per rated kW. Compared to competitor solutions with similar modules or discrete isolated packages (TO220-fullpack) the DC current rating is higher according to **Figure 3**. The diagram shows the DC rating of the IGBT at a case temperature of T_C = 25°C and T_C = 100°C. Nevertheless, junction is operated at 150°C for CIPOS™. The competitor part is also rated up to 150°C, which is the limit also in this comparison. The DC-current of CIPOS™ is higher than the closest competitor by 20% at 25 °C and even 30% at 100°C for the IGBT. The DC current depends on the

output characteristic of the assCIPOSembled IGBT and its thermal resistance R_{thJCI} . So both a very good electrical and thermal performance are important to achieve such high values for CIPOS™.

The second solution is a discrete solution which bases on Infineon IKA06N60T. This is a component in TO220 fullpack. It is easy to see, that these devices provide a similar DC rating than the closest competitor. However, this discrete solution is not considered further on in this application note.

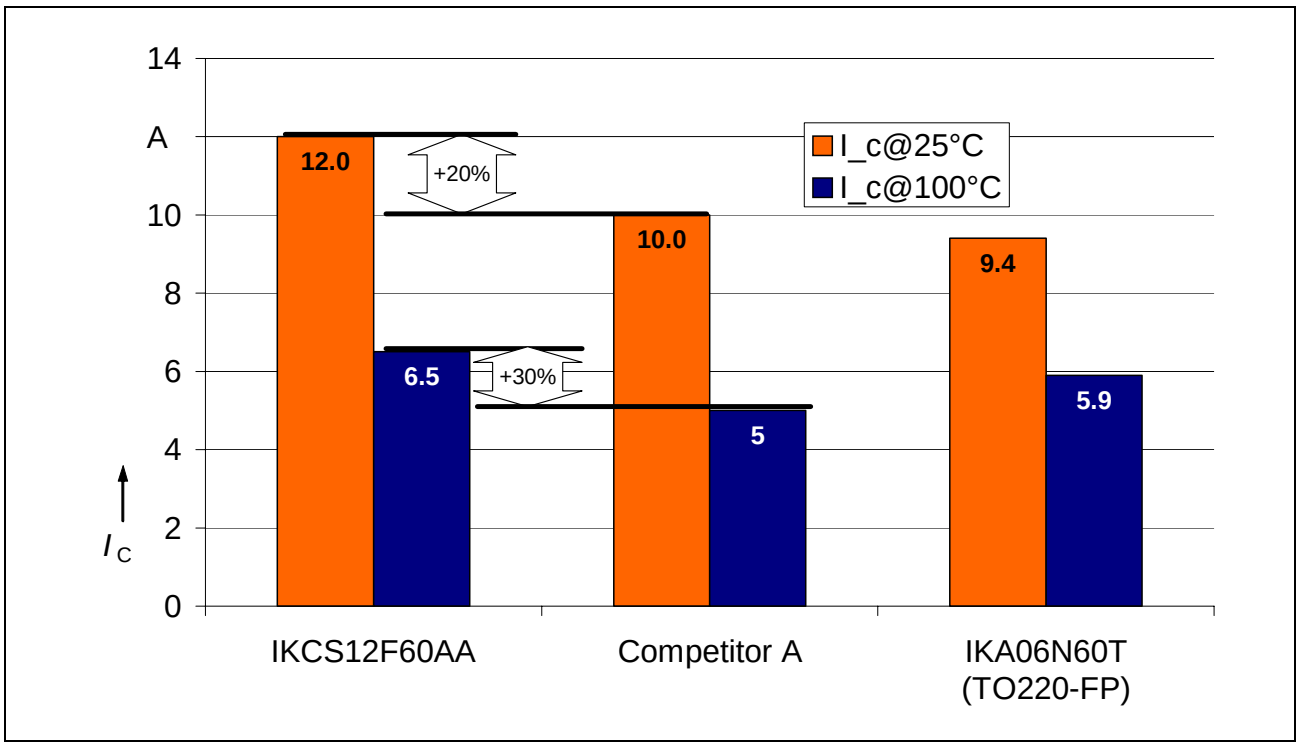

Figure 3 DC current rating of CIPOS™, competitor and Infineon Fullpack solution

2.2 Mold Compound Characteristic and Creepage Distance at Pins

The performance of the mold compound is essential for calculating the required creepage distances between the pins. The effective parameter is the socalled comparable tracking index (CTI). On basis of the CTI, one can look up and calculate the creepage distance for a given application according to the standards, such as IEC 60664 **[1]** or IEC 60335 **[2]** and others including their amendments. The mold compound of CIPOS™ has a CTI > 600. Common discrete devices usually have a CTI of approximately 300 to 400, which the applicable working voltage. This is a further advantage of CIPOS™. CIPOSCIPOS™ provides a creepage distance of minimum 2.88 mm. This is sufficient for home appliances such as washing machine, vacuum cleaner or air conditioner which are energized from directly from the mains up to 230 V +/- 15%. The creepage distance is even capable of system having a active harmonic filter, e.g. a active boost PFC, which boosts up the working voltage to approximately 400 V.

3 IGBT and Diode Technology

3.1 IGBT

The assembled IGBT-chips in the IKCS12F60AA are identical to IKP06N60T **[3]**. They refer to Infineon´s TRENCHSTOP® technology. This is the latest non-punch-through (NPT) technology and is particularly developped for consumer drive applications. The IGBT assembled in the CIPOS™ module are rated for a maximum junction temperature of T_J = 150°C. Please refer to **[4]** for further information.

3.1.1 Short Circuit Capability

The occurrance of short circuit generates immediately a large amount of heat, which is almost entirely dissipated in the silicon chip.

The 600V TRENCHSTOP® IGBT is specified with a short-circuit robustness up to t_{SC} = 5 µs at T_J = 150°C, V_{GE} = 15 V and V_{CC} = 400 V. Please note here, that the reduction of the short circuit withstand time to 5 µs is not an indicator of reduced short circuit robustness of the TRENCHSTOP® technology. Instead it is a well chosen operational point on a trade-off curve between device performance (i.e. losses under operation conditions) and short circuit withstand time.

In order to understand short circuit capability properly, the known destruction mechanisms shall be discussed. There are principally three mechanisms of short circuit destruction known:

a) destruction during turn-off due to a latch-up which is related to the device over-temperature,

b) destruction during the current pulse (current destruction mode) which is not related to the device temperature. Up to now this destruction mode is not fully understood but design measures are known to avoid this kind of destruction mode,

c) destruction after a successful turn-off (energy destruction) due to thermal run-away of the device as a consequence of the dissipated energy within the pulse. This destruction mode obviously largely depends on the device temperature prior to the short circuit.

With 600 V TRENCHSTOP®-IGBT exclusively the destruction mode c) can be observed, demonstrating the robust and latch-up free device design. **Figure 4** shows a non-destructive short circuit pulse of IKCS22F60AA at a supply voltage of V_{CC} = 15 V. Note that the waveforms show conditions well above the specified short circuit capability.

The above discussion clarifies that once the IGBT technology is short circuit robust the further adjustment of a short circuit withstand time is a matter of definition. State-of-the-art short circuit detection methods are fast enough to recognize and turn off a short circuit within 5 µs. Therefore the specified short circuit withstand time has been set to 5µs in order to provide products with the best price-performance ratio achieving the biggest advantage for the user.

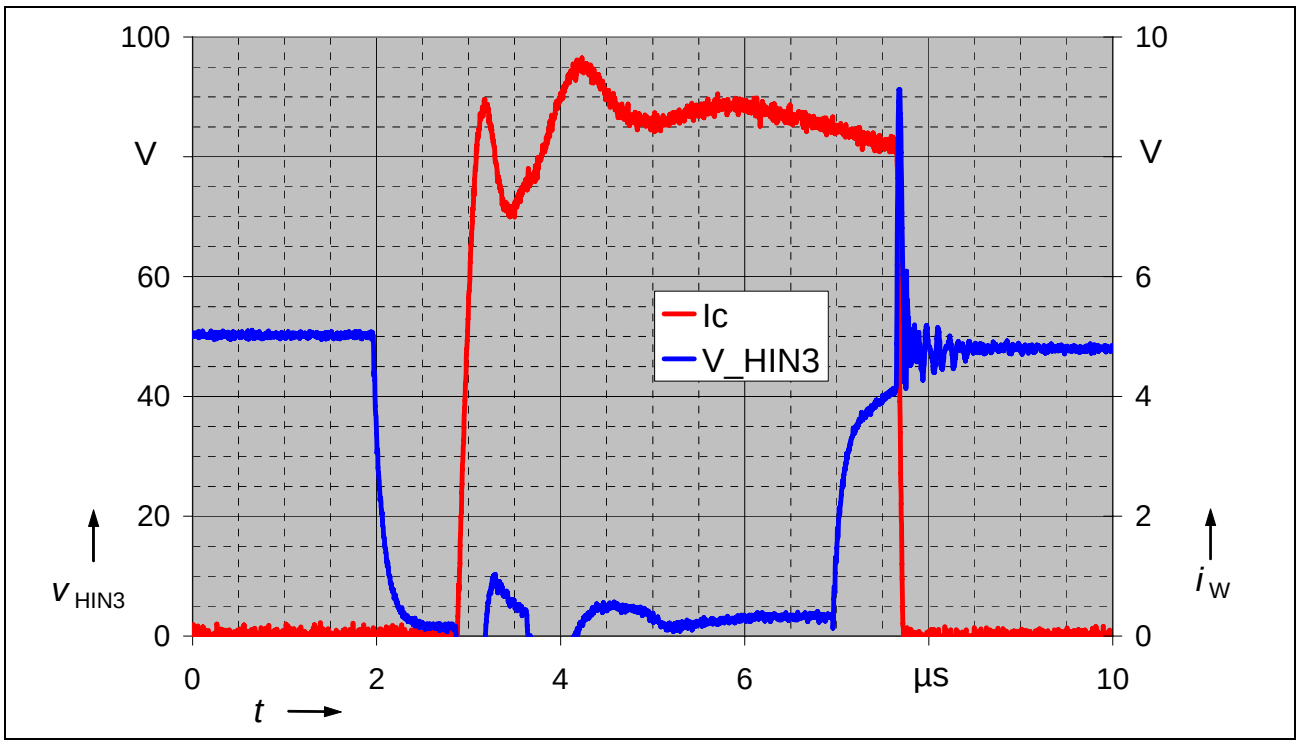

Figure 4 Short Circuit of IKCS22F60T (t_{SC} = 5µs, V_{CC} = 15 V, T_J = 100 °C)

3.2 Diode

The diode technology is optimised in order to support the IGBT in best way in a range of the switching frequency from 5kHz to 16 kHz. This is shown in [5]. Particularly in the upper portion of the switching frequency range, the combination of the used EmCon-technology and TRENCHSTOP®-technology provides much lower overall losses.

4 Control Section

4.1 Input signals ($\overline{\text{LIN}}$, $\overline{\text{HIN}}$)

The input signals can be either TTL- or CMOS-compatible. The logic levels can go down to 3.3V. The maximum input voltage of the pins is internally clamped to 10.5 V. However, the recommended voltage range of input voltage is up to 5V. The control pins LIN and HIN are active low.

They all have an internal pull-up structure with a pull-up resistor value of nominal 70 kΩ. The resistor is not subject of the device test and may vary. The integrated pull-up resistors are designed to pull up the internal structures, so that the IC controls a safe state of CIPOS™. An external pull-up circuit is therefore probably necessary. Nevertheless, it is necessary to check, if the connected devices such as microcontrollers are not causing a turn-on signal during exceptions such as reset. The Infineon controller XC866 I/O-pins are configured as inputs during reset and therefore the CIPOS™ is able to pull up the µC pins. Harsh environments in terms of EMI may need a C-filter close to the input pins according to **Figure 5**.

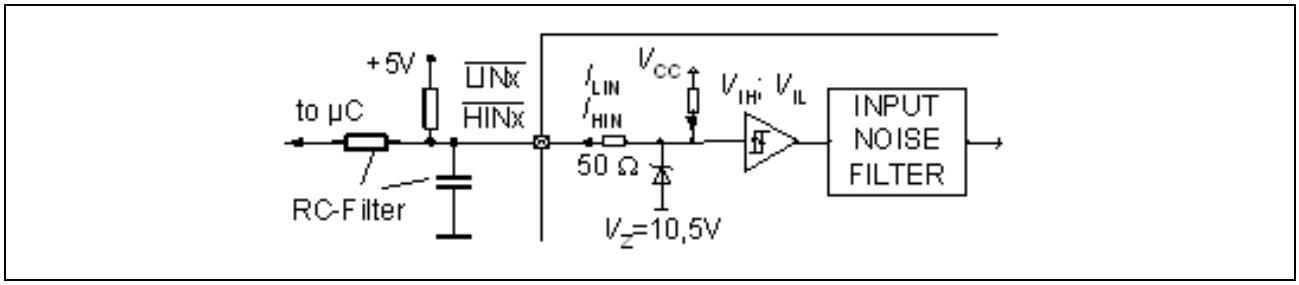

Figure 5 C-filter of input signals and pull-up circuit

The input noise filter suppresses short pulses and prevents the driven IGBT from excessive switching losses. The input noise filter time at LIN for turning on and off the IGBT and at HIN for turning on the IGBT is typically t_{FILIN} =270 ns. This means, that an input signal must stay on its level for this period of time in order that the state change is processed correctly according to **Figure 6** and **Figure 7** repectively.

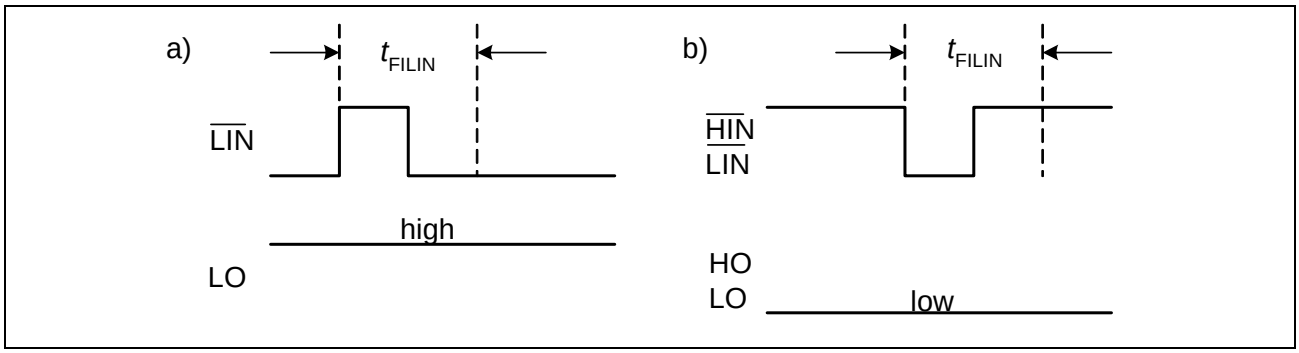

Figure 6 Timing Diagram for Input Filter Characteristic

The turn-off of the highside IGBT is processed, when a HIGH-level signal at the pins /HIN occurs for longer than typically t_{FILIN1} =200 ns the according to b) of **Figure 7**. Otherwise the change in the status of the input signal /HIN will be skipped.

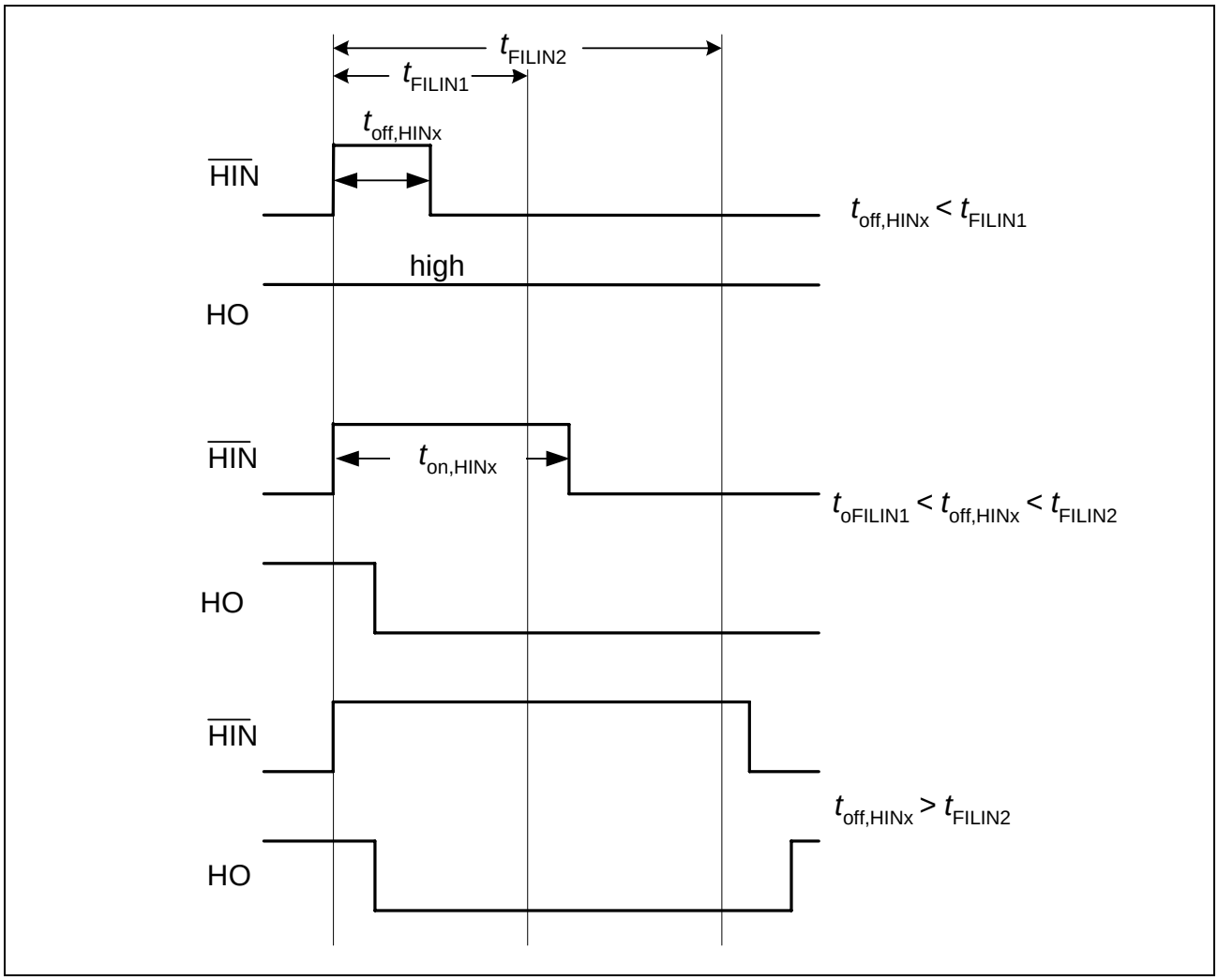

Figure 7 Timing Diagram for Input Filter Characteristic

A full pulse is transmitted , if it is longer than t_{HIN} = 350 ns typically. However, it is recommended to stay above a minimal pulse duration of 1 µs. This means, that also an external RC-filter is not necessary in most cases.

4.2 Deadtime turn-off and turn-on

It is mandatory to establish a deadtime between the turn-off of a high side transistor and the following turn-on of a low side transistor. The driver IC inside the CIPOS™ package is generating such a deadtime of typically DT = 325ns. This is a feature, which helps to prevent short circuit due to overlapping of gate voltage at the gate pins of the IGBT.

However, the ingrated IGBT have specific delay times for turn-on and turn-off. They are not symmetric. The turn-off delay time for IKCS12F60AA is typically $t_{d(off)}$ = 400 ns,

whereas the turn-on delay time is typically $t_{d(on)}$ = 20 ns. The fall and rise times of the IGBT have to be considered as well. The fall time for IKCS12F60AA is typically t_f = 70 ns and the rise time is typically t_r = 20 ns.

The resulting time of the IGBT for turning it totally off is therefore $t_{d(off)}$ + t_f= 400 ns + 70 ns = 470 ns. The corresponding delay for turning it on is $t_{d(on)}$ + t_r= 20 ns + 20 ns = 40 ns. The difference of both is Δt = 470 ns - 40 ns = 430 ns, which is larger than the deadtime of the driver IC (DT = 325 ns). The generated deadtime by the driver IC is therefore not sufficient to avoid a short circuit at all conditions. The mentioned intervals $t_{d(off)}$, $t_{d(on)}$, t_f and t_r are generally increasing for IGBT with higher current ratings. Therefore the difference Δt is also larger for IKCS22F60AA. **Figure 8** shows the input signals (red and green) as well as the corresponding phase output voltage (light blue) and the phase output current (dark blue) for IKCS22F60AA. It can be seen that a deadtime of approx. 440 ns is not sufficient in order to avoid a shoot through for about 250 ns.

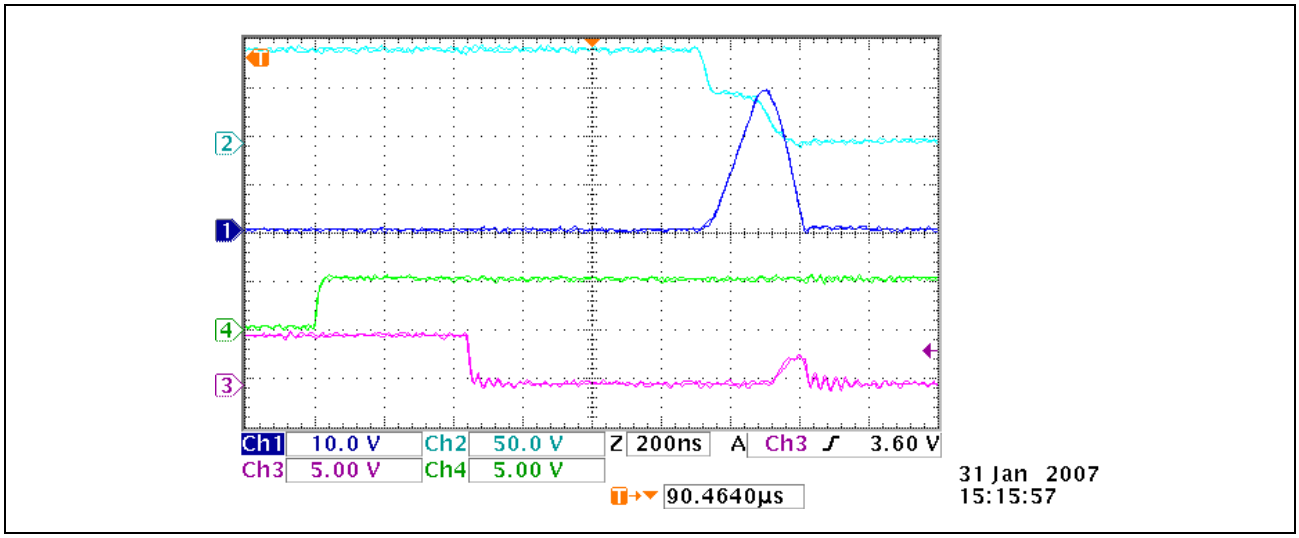

Figure 8 Bad Timing of Input Signals

This means, that the deadtime must be set by the microcontroller. A minimum deadtime of 1 µs for IKCS12F60xx is recommended in order to avoid short term short circuit of a half bridge leg.

4.3 Bootstrapping

Bootstrapping is a common method of pumping charges from a low potential to a higher one. With this technique a supply voltage for the floating highside sections of the gate drive can be easily established according to **Figure 9**. It is only the effective circuit shown for one of the three half bridges. The current limiting resistor RLim is connected to each of the three bootstrap diodes in the module. Please refer to the datasheet in order to see the internal schematic.

The first puls of transistor T2 will force the potential of pin VS to GND. The resulting d*v*/dt leads to a displacement current i_{BS} into the capacitor C_{BS1}. The current i_{BS} is a pulse current and therefore the ESR of the capacitor C_{BS1} must be very small in order to avoid

losses in the capacitor, that result in lower lifetime of the capacitor. The CIPOS™ provides the pin VB, so that additional external capacitors can be used according to C_{BS2} in **Figure 9**. The integrated capacitor is C_{BS1} = 100nF.

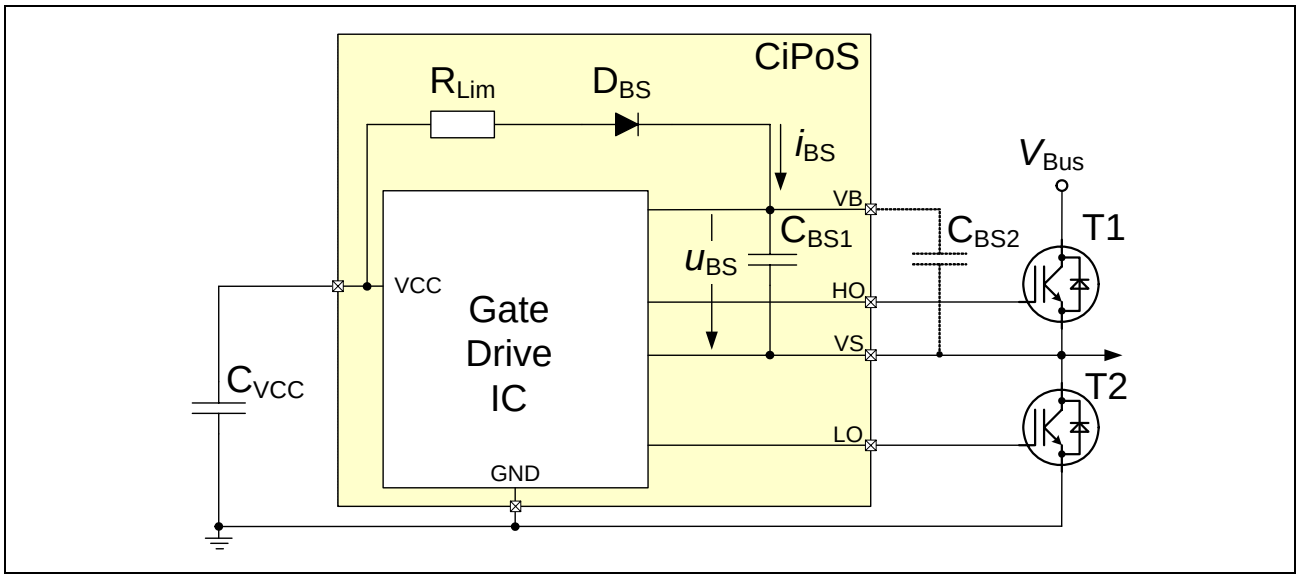

Figure 9 Bootstrap circuit for the supply of a highside gate drive

This pin is on high potential again after transistor T2 is turned off. But now the bootstrap diode D_{BS} blocks a reverse current, so that the charges on the capacitor remain the same. The bootstrap diode also takes over the blocking voltage between pin VB and VCC. The voltage of the bootstrap capacitor can now supply the highside gate drive sections.The voltage of bootstrap capacitor is approximately

$$v_{BS} \approx V_{CC} - V_{FBS} \tag{1}$$

A current limiting resistor R_{Lim} reduces the peak of the pulse current during the turn-on of transistor T2. The pulse current will occur at each turn-on of transistor T2,so that with increasing switching frequency the capacitor C_{BS1} and C_{BS2} are charged more frequently. Therefore a smaller capacitor is suitable at higher switching frequencies. A low leakage current of the highside section is very important in order to keep the bootstrap capacitors small. The bootstrap capacitor is discharged by two effects: The leakage current and the gate charge of the transistor to be turned on. The calculation of the bootstrap capacitor results in

$$C_{BS} = \frac{i_{QBS1} \cdot t_P + Q_G}{\Delta v_{BS}} \tag{2}$$

with i_{QBS1} being the quiescent current of the highside section, t_P the switching period, Q_G the total gate charge and Δv_{BS} the voltage drop at the bootstrap capacitor within a switching period. Please note here, that **Equation (2)** is valid for continous switching according to the switching frequency. The use of space vector modulations can cause

periods up to 60° (electrical), in which no switching of the low side transistor of a half bridge occurs. This effects the bootstrap capacitor size, especially for low output current (motor current) frequencies. In this case the variable t_P must be set to the longest period of no switching. **Figure 10** shows the curve corresponding to **Equation (2)** for a con-tinuous sinusoidal modulation, if the voltage ripple Δv_{BS} = 0.1V. The recommended boots-trap capacitance is therefore in the range up to 4.7µF for most switching frequencies.

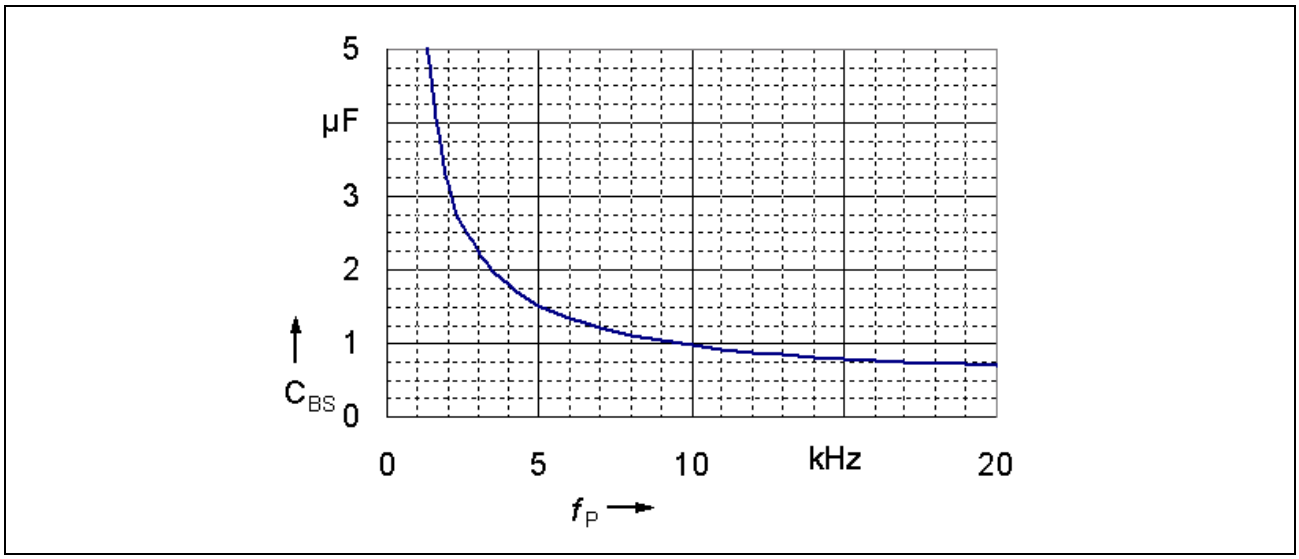

Figure 10 Recommended size of the bootstrap capacitor as a function of the switching frequency f_P at a supply voltage of V_{DD} = 15V

Please note, that one of the limiting factors of the bootstrap capacitor design is the power capabilities of the bootstrap resistor. There are different ways to reduce the stress of the resistor, such as loading the capacitance phase by phase sequentially with a period of approximately 50ms between each phase being charged. **Figure 11** shows the max. bootstrap capacitance for sequentially charging the bootstrap capacitances.

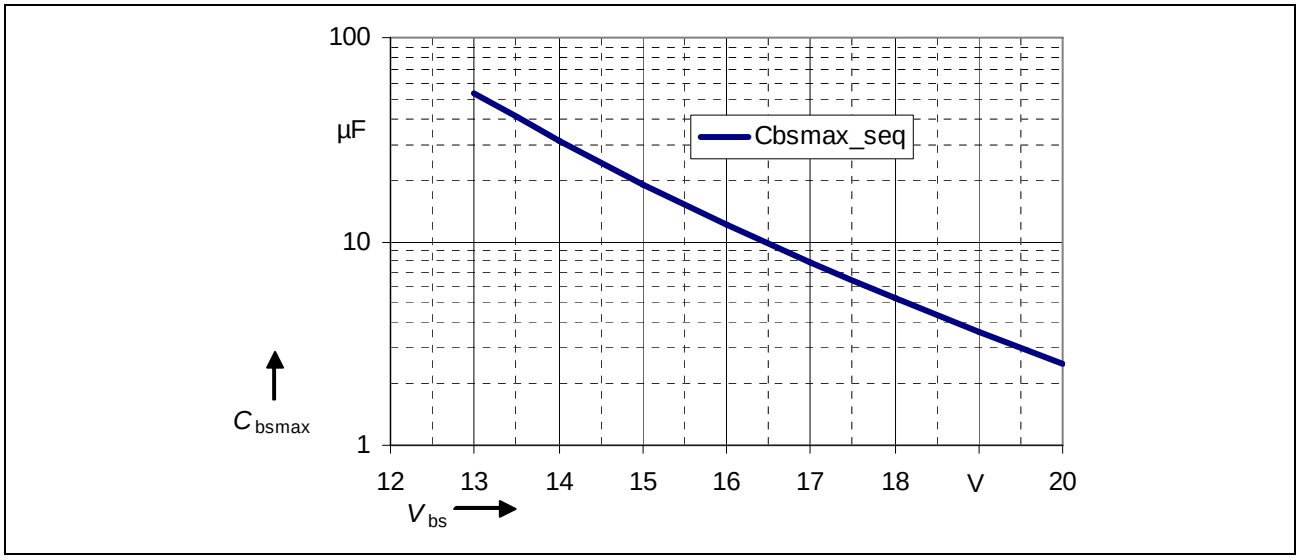

Figure 11 Max. bootstrap capacitance vs. supply voltage for sequential charge

It is necessary for the sequential charging of the bootstrap capacitors, that the turn-on period of the low side transistors is a multiple of the charging RC time constant. It should be larger than 5*RC in order to ensure, that the capacitors are properly charged.

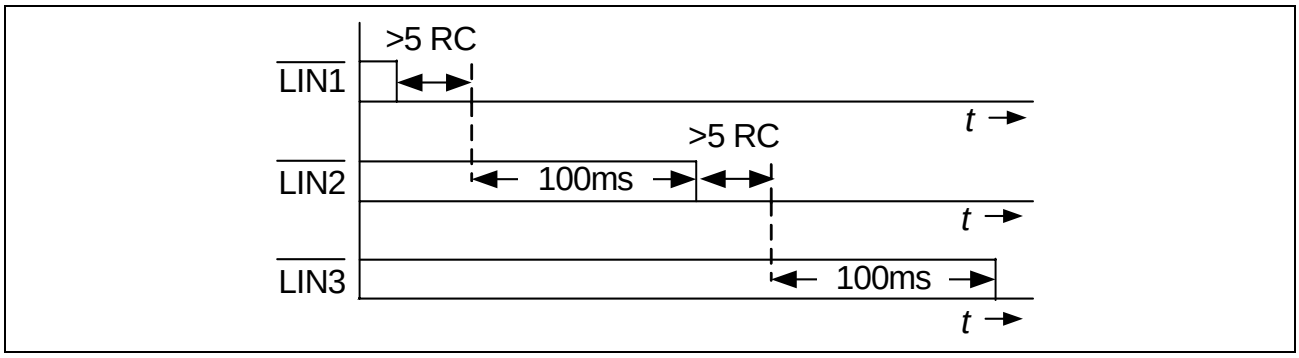

Figure 12 Possible charging scheme for bootstrap capacitors

4.4 Overcurrent Protection (ITRIP)

The overcurrent protection is a major feature of IKCS12F60AA. It is realised by accessing the shunt signal R_{SH} according to **Figure 14**. The CIPOS™ stops operation as soon as the voltage level at pin ITRIP is higher than typcally $V_{IT,TH+}$ = 0.45 V. This corresponds to a current level of

$$I_{ITRIP} = \frac{V_{IT,\,TH+}}{R_{SH}} \quad (3)$$

An internal comparator is triggered and sets a latch flip-flop. This flip-flop inhibits the output sections of both highside and lowside transistors. After triggering the ITRIP-comparator, a current source charges a RC-network. The CIPOS™ restarts operation after approximately 5ms.

The very low threshold of the ITRIP comparator allows to feed the shunt signal directly into the ITRIP pin. As a result, the voltage divider is not necessary. A RC-filter, which attenuates voltage spikes in the shunt signal, is recommended here instead.

A voltage divider is not necessary here, because the trigger level of 0.45 V is low enough, in order to directly connect the output of the RC-filter with pin ITRIP.

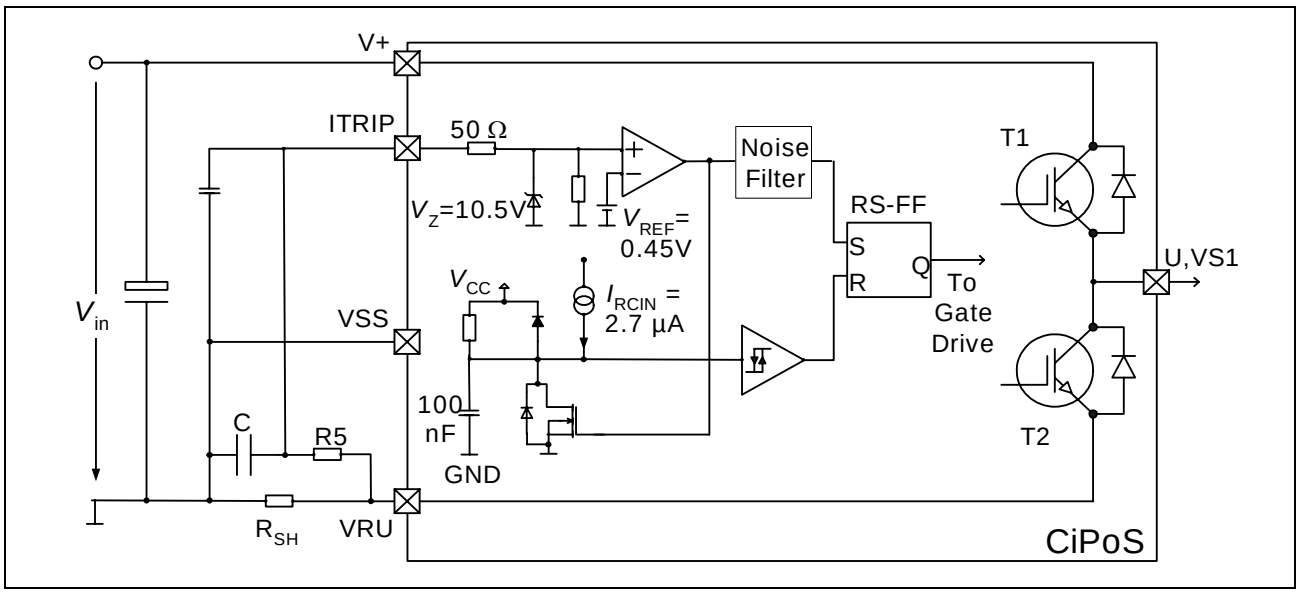

Figure 13 Structure of the overcurrent protection and overcurrent recovery

The ITRIP pin is internally clamped by internal zener diode to 10.5 V.

4.5 Supply Voltage (VCC) and Undervoltage Lockout (UVLO)

The supply voltage covers a range up to maximum 20 V. Above this value an internal clamp circuit will limit this parameter to 20 V. It is necessary to assure by design, that the voltage does not increase further than 20 V, because the activation of the internal clamp causes local losses, which can lead to a destruction of the device. Temporarily higher voltages can occur, if the auxiliary (AUX-) power supply is not operating properly or if the supply voltage of CIPOS™ is not directly controlled by the AUX-supply. The recommended operating range is up to 17.5V, because there is still a good margin the clamp limit.

CIPOS™ will move from standby operation into normal operation, when the supply voltage at pin VCC is higher than 12 V typcially according to **Figure 14**. The beginning of the pulse operation will pump charges into the bootstrap capacitor, so that the bootstrap voltage will rise accordingly. As soon as the bootstrap voltage is higher than 12 V also the highside sections of CIPOS™ are clear for operation.

The CIPOS™ operates in normal mode down to a supply voltage of 10.3 V for both the bootstrap voltage and the lowside supply voltage. This is important in order to prevent the IGBT from too low gate voltage, which could damage the IGBT due to excessive losses.

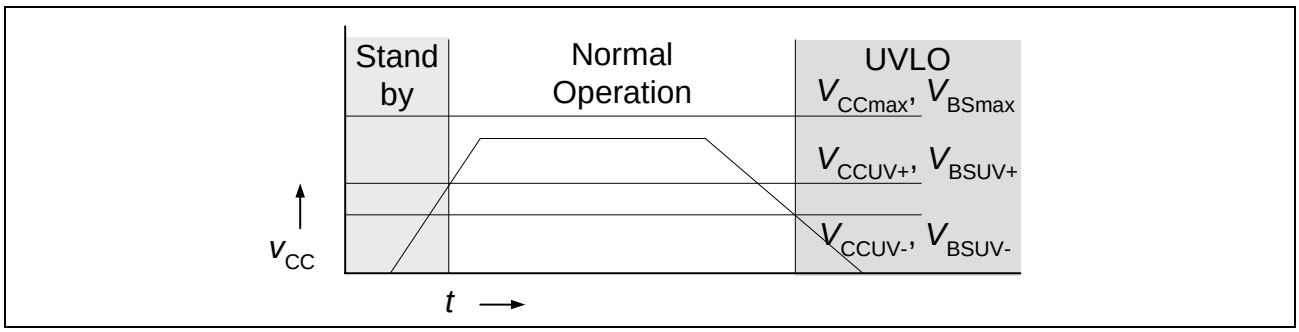

Figure 14 Voltage levels for start up and UVLO

4.6 Thermal Protection

The thermal protection is realised with a NTC-resistor according to **Figure 15**. The protection is entirely inside CIPOS™ and the tap of the voltage divider will trigger the comparator, when the voltage reaches $V_{EN,th-}$ = 1.32 V typ. This point represents a temperature at the location of the NTC of 125°C, which is also the maximum operating temperature of the gate drive IC. The NTC is located on the PCB of CIPOS™.

The positive going threshold of the comparator is $V_{EN,th+}$ = 2.1 V typically, which represents a temperature of approximately 110°C. This means that the CIPOS™ must cool down first, before it restarts operation.

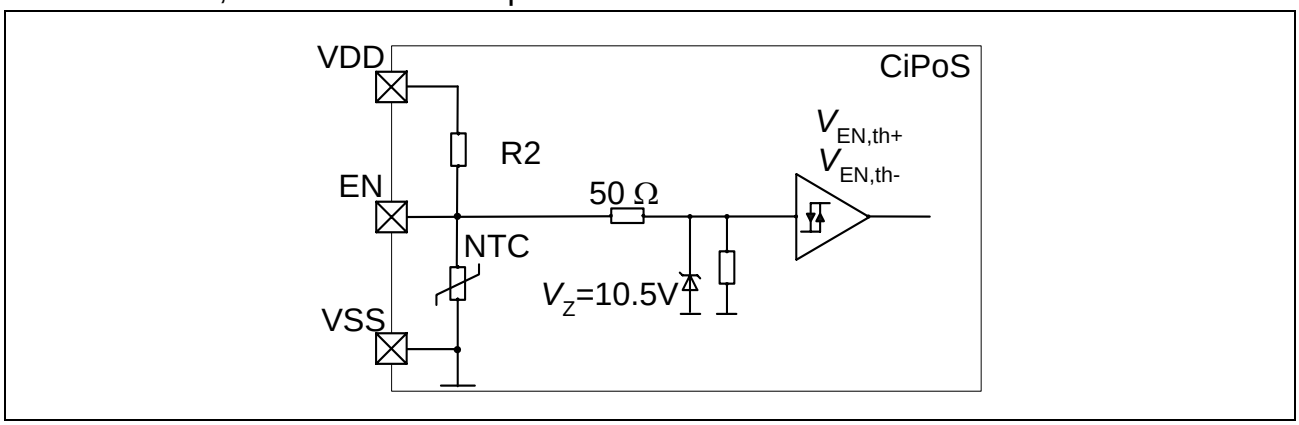

Figure 15 Thermal Protection with NTC

It is important for CIPOS™ to protect the gate drive IC from overtemperature. However, the thermal protection should also protect the power semiconductors from overheating. It is therefore necessary to have a good thermal coupling of the semiconductors to the NTC. A sufficient way of coupling the DCB and the PCB is to choose a heatsink, which covers the complete backside of CIPOS™. This leads to a good heat transfer via the heatsink itself. The reaction time of the NTC is then approximately 150 seconds.

The NTC circuit according to **Figure 15** is dependent on the supply voltage of CIPOS™, because the voltage at the tap varies at a constant temperature, if the supply voltage changes. This means, that also the trigger tempeatureof the overtemperature protection

can vary, if the supply voltage is not constant. The NTC has a typical resistance at 25°C of 100 kΩ and a socalled B-constant of 4250. The resistance of the NTC is therefore

$$R_{NTC}(T) = R_0 e^{B\left(\frac{1}{T}-\frac{1}{T0}\right)} \quad (4)$$

where R_0 =100 kW, B = 4250 K, T0 = 298 K, T is the NTC-temperature in Kelvin. The overall characteristic of the voltage at pin EN is given in **Figure 16**

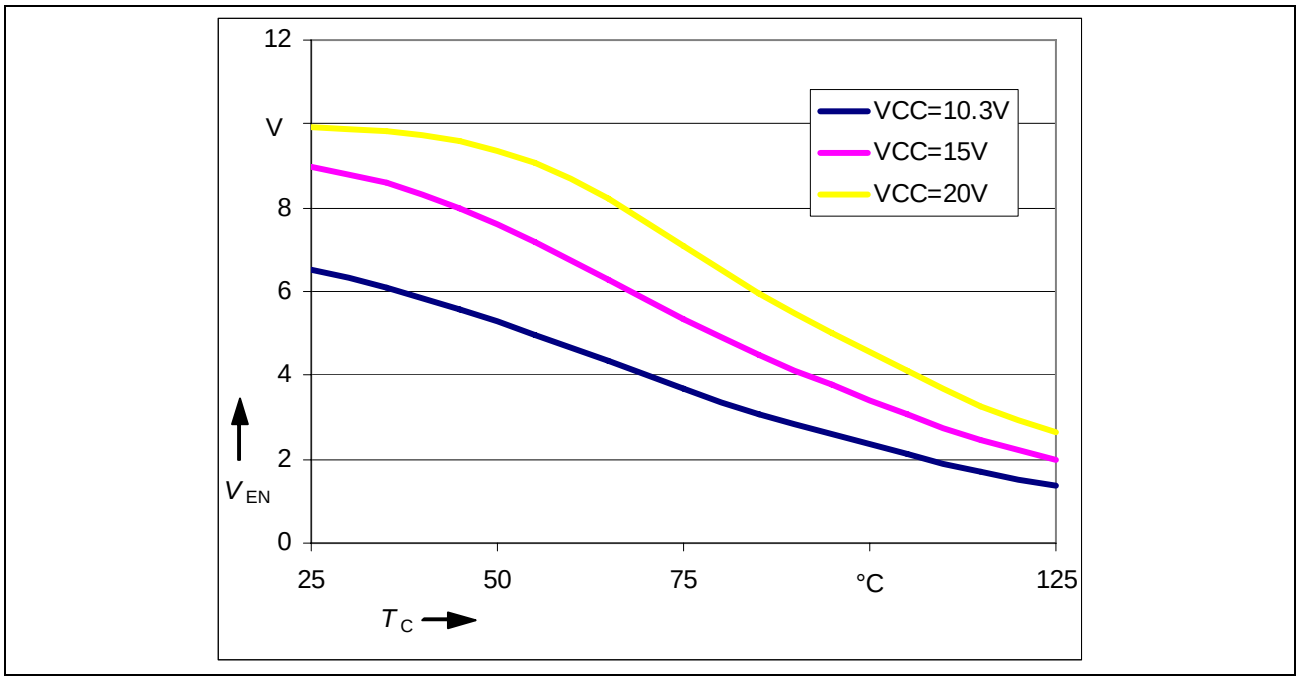

Figure 16 Typical characteristic of pin EN as a function of temperature

4.7 HF Bypassing of DC-link

A bypass capacitor for shorting the high frequency portion of the currents, which occur due to the switch mode operation of the inverter is recommended. The capacitor should be located as close to the pins “V+” and “VSS” as possible. This results in small parasitic inductances in respect of the high-side DC-link track as well as the emitter-side tracks. It also keeps the disturbance in terms of EMI concentrated close to the CIPOS™ module.

5 Summary of Used Nomenclature

Physics:

General identifiers:

A .....cross area
b, *B* .....magnetic inductance
d, *D* .....duty cycle
f.....frequency
i, *I* .....current
N .....number of turns
p, *P* .....power
t, *T*.....time, time-intervals
v, *V*.....voltage
W .....energy
η.....efficiency

Special identifiers:

A_L..... inductance factor
$V_{(BR)CES}$.. collector-emitter breakdown voltage of IGBT
V_F..... forward voltage of diodes
V_{rrm} ..... maximum reverse voltage of diodes

big letters: constant values and time intervals
small letters: time variant values

Components:

C .....capacitance
D .....diode
IC .....integrated circuit
L ..... inductance
R..... resistor
TR..... transformer

Indices:

AC.....alternating current value
DC.....direct current value
BE.....basis-emitter value
C .....Collector value
CS.....current sense value
E .....Emitterr value
G .....Gate value
OPTO..optocoupler value
P .....primary side value
Pk.....peak value
R..... reflected from secondary to primary side
S .....secondary side value
Sh .....shunt value
UVLO..undervoltage lockout value
Z.....zener value
fmin..... value at minimum pulse frequency
i .....running variable
in .....input value
max .....maximum value
min .....minimum value
off .....turn-off value
on .....turn-on value
out .....output value
p .....pulsed
rip .....ripple value

1, 2, 3 .....on-going designator

6 References

[1] International Electrotechnical Commission: IEC 60664-1 Insulation coordination for equipment within low-voltage systems Part 1: Principles, requirements and tests; International Standard; IEC, Geneva, Switzerland.

[2] International Electrotechnical Commission: IEC 60335-1 Household and similar electrical appliances - Safety Part1: Part 1: General requirements; International Standard; IEC, Geneva, Switzerland.

[3] .Infineon Technologies: IKP06N60T; Datasheet; Infineon Technologies, Germany, 2006.

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