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## Surge Current, I<sup>2</sup>t – Value and Short - Circuit Protection of High Power Semiconductors.

According to DIN IEC 60747 the maximum rated surge current is the maximum allowable non periodical, sinusoidal 50 Hz or 60 Hz half wave, without any following voltage and/or current stress. The  $I^2t$  – value is the maximum allowable value of the time – integral over this current, related to the indicated junction temperature.

The semiconductors may lose, when stressed with maximum rated surge current, their blocking capability completely or partly, till the junction temperature will have decreased to the temperature range permitted for continuous work. This stress may be repeated at the earliest after several seconds and should occur only occasionally at a limited pulse number during the entire actual operating time of the semiconductor.

Maximum rated surge forward current and maximum load integral are used to design the over-current protection of diodes and thyristors. As pure sine-wave currents in practice do not occur, the conversion to similar current forms of about equal pulse width can be made by the  $l^2t$  – value.

One differentiates between the following typical failure modes:

- Outside short-circuit on the load side.
- Internal short-circuit caused by a defect of a semiconductor, or by misfiring of a thyristor.

## **Protection concepts:**

### 1) Super fast semiconductor fuses

These fuses, arranged in the branch or in the arm, disconnect within one half wave. Their  $l^2t$  - value must be lower than that of the semiconductor that has to be protected. During the current rise first the cartridge of the fuse melts, the resulting arc afterwards is put out by the surrounding filling material, usually quartz sand.



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The fuses react within 3 to 5 ms (Fig. 1), therefore in former times also semiconductor values were indicated for that time periods. Because of better utilization, however, the design was changed to 10 ms values at maximum junction temperature. Because of the higher temperature dependence of the fuse as compared to the semiconductor, the unsecured area is fairly small.

During the erasing process the fuse causes a switching – voltage, the height of which depends on the design of the fuse – cartridge and the repetitive voltage. Such voltage peaks may not exceed the surge voltage of the semiconductors, in order not to endanger blocking elements in the circuit.

For the sake of the completeness it is mentioned that there are also concepts, with which the fuses do not protect the semiconductors but have the task only to separate defect semiconductors from the electric circuit. This is the case with high current converters, which may not be switched off during operation, e.g. aluminum melts.

**2) Direct current high-speed circuit-breakers** with electro-dynamic release switch off in the case of short-circuits within a few milliseconds. Because of the high costs they are, however, used in exceptional cases only.

**3) Crowbars** are mainly used in voltage source inverters with semiconductors that can be turned – off (IGBT, GTO, and GCT). If the link voltage exceeds a defined protection level, the crowbar is fired and unloads the link capacity. The discharge surge current is led into the arms of the inverter either across a special ring around diode or across the freewheeling diodes.

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power electronics in motion

#### 4) Line circuit-breaker

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The semiconductors must lead the short circuit current till the circuitbreaker switches off the line. That happens usually after 3 to 5 half waves in case of high power installations. The current form usually is a (1-cos) function, the pulse width of which depends on the circuit data. During this time the semiconductors are loaded with reverse voltage. The thyristors have to be fired in each current zero crossover (Fig. 2).





5) Gate barrier with thyristors suppresses the ignition pulses when exceeding a defined current release value. The thyristors are stressed with one current - half wave (Fig. 3) with following reverse and forward blocking voltage. This anticipates that the semiconductors still have sufficient reverse - and blocking voltage capability.





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From the variety of possible protection concepts it becomes clear that the indication of one value for a sine half wave by the semiconductor manufacturer is not sufficient. Depending on the concept, data are necessary, which require additional tests carried out at suitable equipment.

## Semiconductor Design and Surge Current

Besides the design of the active area, there is a basic dependence of the maximum rated surge forward current on the  $V_T - Q_r$  adjustment and the silicon thickness of the semiconductor. The silicon thickness is defined by the required blocking capability. Apart from that parameter, the heat dissipation from the junction of the silicon in the short time range is of big influence.

The alloying process of a silicon wafer onto a molybdenum carrier disk, as it was common in former times, proved as unfavorable, particularly in case of large area semiconductors. Strong deflections of the pellets resulted from this high temperature process. To avoid this effect, eupec developed a low temperature joining process which leads to a stable connection between silicon wafer and molybdenum carrier disk.

eupec process NTV (low temperature joining process)

In this case, silicon and molybdenum are connected under high pressure at about 240°C by using different metals (Fig. 4). eupec uses this process for high blocking voltage devices and semiconductors with large active areas.



Fig. 4





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### Surge current values:

The present data sheets will be changed as per PCN 2005-06 dated 2005-03-08 (data sheets for high-power thyristors and diodes) to the conditions given in these tables. Only the regarding data sheet value are valid. **Rectifier diodes:** 

Туре	Pellet	V <sub>RRM</sub>	T <sub>vj m</sub>	I <sub>FSM</sub>	I <sub>FSM</sub>	I <sub>FSM</sub>	Note
	Ømm	kV	С°	Sine 10ms	Sine 10ms	damped sine	
				T <sub>vj m</sub>	25°C	0,25ms, 125°C	
D4201N	76	2,2	160	73,5 kA	88 kA		
D3501N	76	4,2	160	56 kA	63 kA		
D2201N	65	4,5	140	35 kA	38 kA	150 kA	Crowbar
D6001N	101	5	160	~ 110 kA			
D711N	38	6,8	160	10,5 kA	12,5 kA		
D1481N	55	6,8	160	24,5 kA	28 kA		
D3001N	76	6,8	160	53 kA	57 kA		
D3041N							
D471N	38	9	160	10 kA	11 kA		
D2601N	76	9	160	50 kA	52 kA		

### GCT freewheeling diodes:

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Туре	Pellet	V <sub>RRM</sub>	T <sub>vj m</sub>	I <sub>FSM</sub>	Note
	Ø mm	kV	°C	Sine 10ms T <sub>vj m</sub>	
D911SH	65	4,5	140	17 kA	Different V <sub>F</sub> – Q <sub>r</sub> window compared to D1031SH
D1031SH	65	4,5	140	23 kA	
D1121SH	76	4,5	140	17,5 kA	Different V <sub>F</sub> – Q <sub>r</sub> window compared to D1331SH
D1331SH	76	4,5	140	28 kA	
D931SH	65	6,5	140	16 kA	
D1131SH	76	6,5	140	22 kA	
D1951SH	101	6,5	140	44 kA	

#### GTO freewheeling diodes:

Туре	Pellet	V <sub>RRM</sub>	T <sub>vj m</sub>	I <sub>FSM</sub>	I <sub>FSM</sub>	I <sub>FSM</sub>	I <sub>FSM</sub>
	Ømm	kV	°C	Sine 10ms T <sub>vj m</sub>	Sine 10ms 25°C	Sine 0,68 ms T <sub>vj m</sub>	damped Sine 0,25ms, 125°C
D721S	55	4,5	125	18 kA	20 kA	50 kA	
D1251S	55	4,5	140	18 kA			90 kA
D1461S	65	4,5	140	28 kA			
D921S	65	4,5	140	28 kA		> 75 kA	
D1381S	65	4,5	140	28 kA			

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### GTO snubber diodes

Туре	Pellet	V <sub>RRM</sub>	T <sub>vj m</sub>	FSM	Note
	Ø mm	kV	°C	Sine 10ms T <sub>vj m</sub>	
D291S	33	4,5	125	4,5 kA	
D371S	38	4,5	125	6 kA	snubberless
D801S	55	4,5	125	14 kA	snubberless
D841S	55	4,5	125	18 kA	
D901S	65	4,5	125	21,5 kA	snubberless

### Silicon Controlled Rectifiers LTTs (Light Triggered Thyristors)

Туре	Pellet	V <sub>RRM</sub>	T <sub>vj m</sub>	I <sub>TSM</sub>	I <sub>TSM</sub>	I <sub>TSM</sub>	I <sub>TSM</sub>
	Ømm	kV	С°	Sine 10ms	Sine	1HW(1- cos)	3HW(1- cos)
				T <sub>vj m</sub>	10ms	16,5ms, 90°C	16,5ms, 90°C
					25°C	$V_R$ , $V_D$	V <sub>R</sub>
T4003N	119	5,2	120	100 kA	105 kA		
T553N	55	7	120	11,7 kA	12,1 kA		
T1503N	101	8	120	55 kA	57 kA	26 kA	26 kA
T2563N	119	8	120	90 kA	93 kA		

### Silicon Controlled Rectifiers - ETTs (Electric Triggered Thyristors)

Тур	Pel-	V <sub>RR</sub>	T <sub>vi m</sub>	I <sub>TSM</sub>	I <sub>TSM</sub>	I <sub>TSM</sub>	I <sub>TSM</sub>	I <sub>TSM</sub>
	let	м		_		_	_	_
	Ømm	kV	°C	Sinus 10ms T <sub>vj m</sub>	Sinus 10ms 25°C	1HW(1- cos) 16,5ms, 90°C V <sub>R</sub> , V <sub>D</sub>	3HW(1- cos) 16,5ms, 90°C V <sub>R</sub>	5HW(1- cos) 16,5ms, 90°C V <sub>R</sub>
T2101N	76	2,6	125	47 kA	56 kA			
T4771N T4301N	101	2,8	125	91 kA	100 kA			
T901N	55	3,6	125	17 kA	19 kA			
T2001N T1601N	76	3,6	125	41 kA	44 kA	29 kA	29 kA	27 kA
T3801N T3401N	101	3,6	125	87 kA	91 kA	53 kA	53 kA	50 kA
T731N	55	4,4	125	16 kA	18 kA			
T1971N T1401N	76	4,4	125	36 kA	40 kA	19 kA	19 kA	18 kA
T3101N	101	4,4	125	83 kA	87 kA			
T1551N T1451N	77	5,2	125	43 kA	44 kA	24 kA	24 kA	22,5 kA
T2351N T2161N	88,5	5,2	125	54 kA	55 kA	30 kA	30 kA	28,5 kA
T2401N	101	5,2	125	67 kA	70 kA			





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Тур	Pel-	V <sub>RRM</sub>	T <sub>vj m</sub>	I <sub>TSM</sub>	I <sub>TSM</sub>	I <sub>TSM</sub>	I <sub>TSM</sub>	I <sub>TSM</sub>
	let							
	Ø	kV	С°	Sinus	Sinus	1HW(1- cos)	3HW(1- cos)	5HW(1- cos)
	mm			10ms	10ms	16,5ms,	16,5ms,	16,5ms,
				T <sub>vj m</sub>	25°C	90°C	90°C	90°C
						V <sub>R</sub> , V <sub>D</sub>	VR	VR
T3441N	101	5,2	125	79 kA	82 kA	43 kA	43 kA	40 kA
T2851N								
T4021N	119	5,2	125	100	105 kA			
T201N	38	7	125	4,2 kA	4,7 kA			
T501N	55	7	125	12 kA	12,5 kA			
T551N								
T1081N	77	7	125	34 kA	35 kA	17 kA	17 kA	16 kA
T1201N								
T1851N	88,5	7	125	48 kA	50 kA	24 kA	24 kA	22,5 kA
T1651N								
T2251N	101	8	125	65 kA	67 kA			
T1901N								
T2871N	119	8	125	90 kA	93 kA			

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