Definition of the module stray inductance L_s

Fig.1 shows the principle circuit of a half-bridge and the resulting voltage and current waveforms when switching IGBT1. The circuit stray inductance L_σ, shown as a concentrated element, represents all distributed inductances (of capacitors, busbars and IGBT modules) within the commutation loop (striped area).

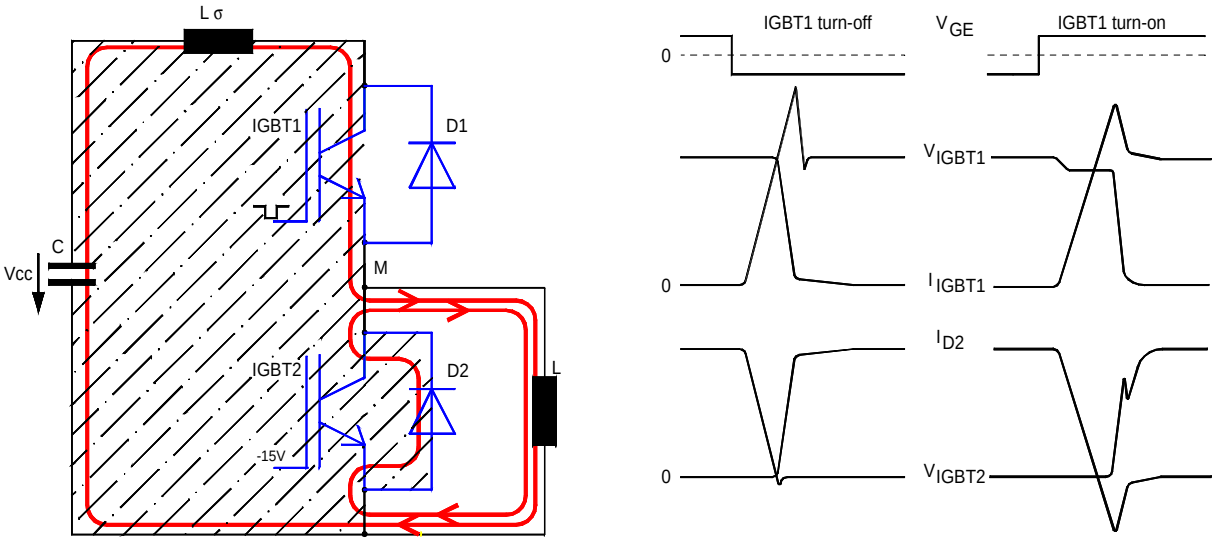

Fig.1: Half-bridge circuit with current and voltage waveforms when switching IGBT1

Due to the changing current a voltage drop of $L_\sigma * di_{off}/dt$ occurs across the stray inductance L_σ. It is overlayed to the DC link voltage V_{CC} and seen as a voltage spike across the turning-off IGBT1. Permissible limits for turn-off current di/dt and overvoltage can be deduced from the RBSOA diagram of the IGBT. This curve (see Fig.2) is valid when the measurement is done through the CE auxiliary terminals. Also a derated curve is given in the data-sheet for measurements at the power terminals, taking into account the internal module stray inductance between main and auxiliary terminals of the module. For dual modules, this diagrams refers to the voltage across one of the both commutating IGBT switches.

For calculations the value for the internal module stray inductance L_s is given in the data-sheets. For single switch modules, this value is the before mentioned stray inductance between main and auxiliary terminal. For dual modules or modules containing several phase legs, this value corresponds to the application relevant effective commutation loop between upper and lower switch. Due to the construction this value is clearly lower than the sum of

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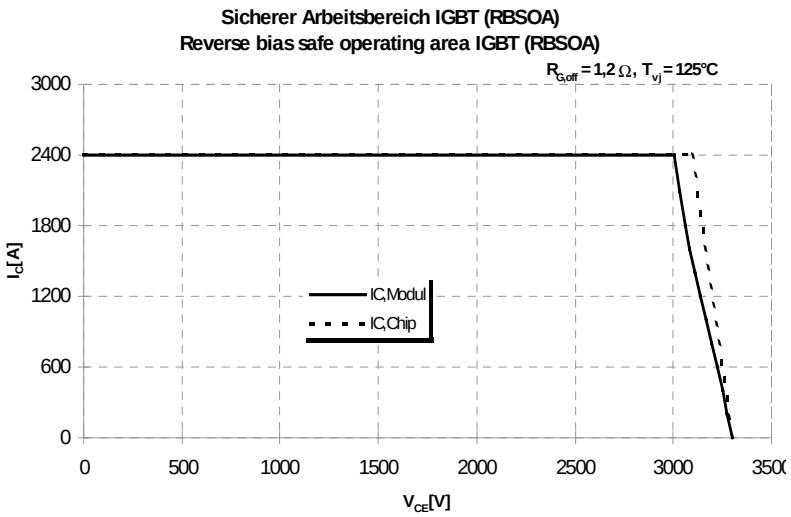


separately determined inductances of upper plus lower arm. In modules with more than one phase leg always the worst case commutation path from plus supply voltage through the phase leg back to minus supply voltage is considered.

Fig.2: RBSOA diagram for FZ1200R33KF2

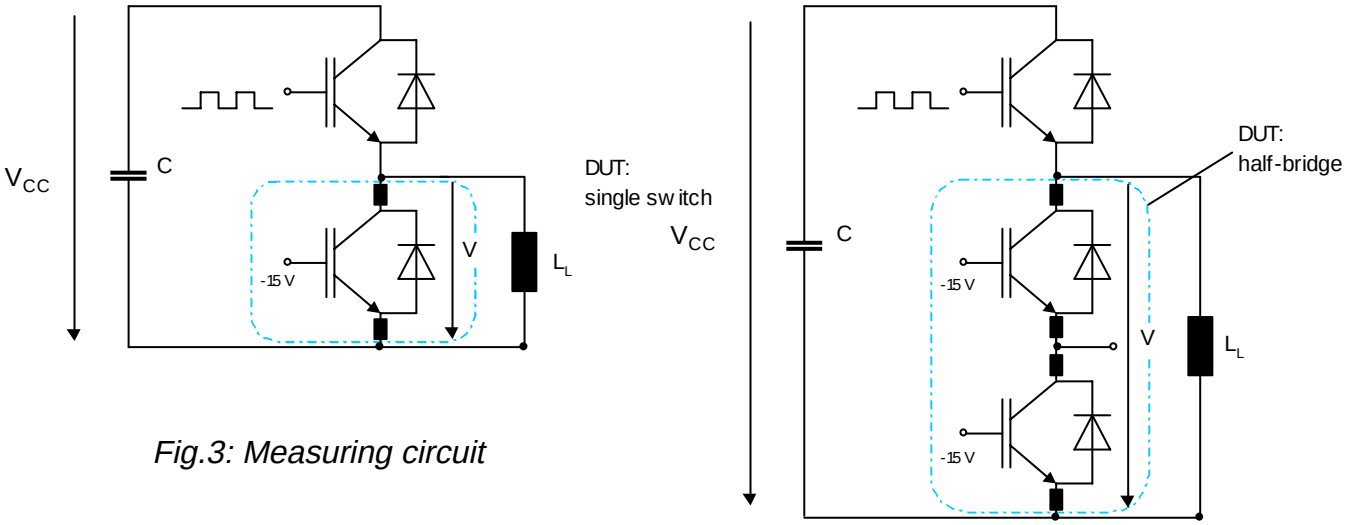
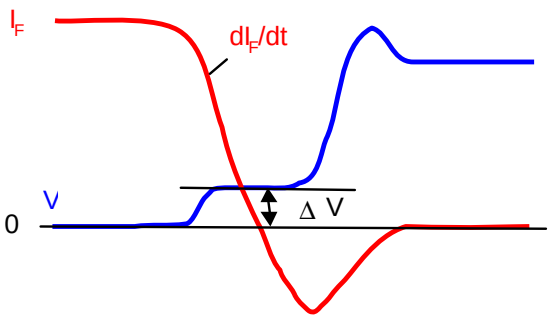


Fig.3: Measuring circuit

The measurement is performed, while the diode turns off. The voltage drop happens at a point of time, where the di/dt is constant and the diode still has no blocking capability. Therefore the voltage drop can only be caused by the module stray inductance. No other effects have to be considered. The module stray inductance is calculated according to $L_S = \Delta V / di_F/dt$.



Dependent on the type designation, the data sheet value for the stray inductance has to be interpreted in the following way:

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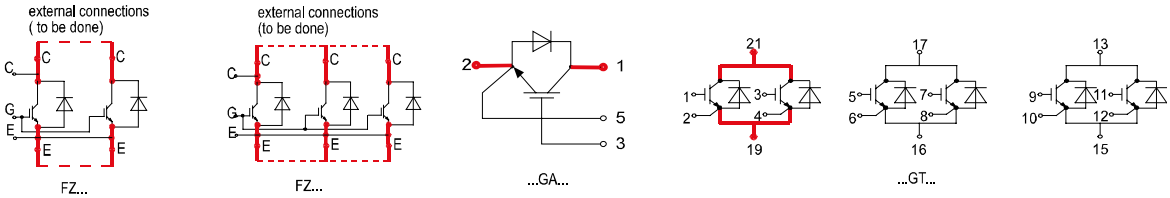
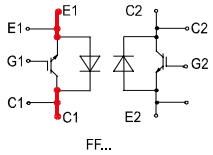
Single modules type FZ... or ...GA... and Tripacks:

The module stray inductance is measured *between the C and E main terminals*.

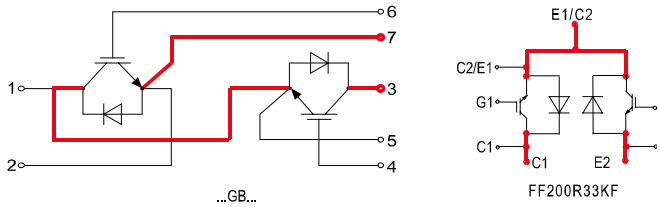


Dual modules type FF... (with exception of FF200R33KF):



These modules contain two independent switches. Given is the stray inductance *between the C and E main terminals of one switch*.

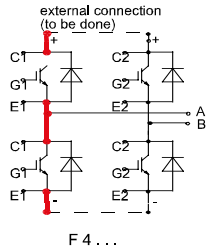
Half-Bridges type ...GB... and FF200R33KF (modules with three main terminals):



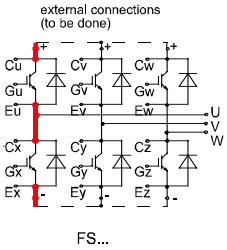
The given data sheet value covers the *full commutation loop between upper and lower switch*, including the inductance between upper C1 and lower E2 terminals.

4-packs type F4-...:

These modules contain two independent phase-legs. The given data sheet value covers the *full commutation loop between upper and lower switch* within one phase-leg, including the inductance between + and - terminals.



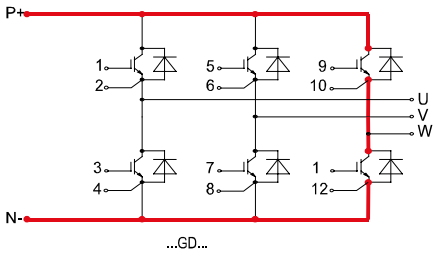
Six pack modules type FS...:



The given data sheet value covers the *full commutation loop between upper and lower switch* within one phase-leg, including the inductance between + and - terminals.

3-Phase full bridges or PIM type ...GD... or ...GP...:

The given data sheet value covers the *full commutation loop between upper and lower switch at the worst position within the module*, containing the full inductance towards the P+ and N- terminals (terminals named „22“ and „24“ with PIM).



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